Report No. 03-68-42

Final Report

DEVELOPMENT OF SILICON NITRIDE AND CERMET RESISTORS FOR USE IN A BINARY COUNTER, METAL INSULATOR FIELD EFFECT TRANSISTOR CIRCUIT

For the Period
1 December 1966—31 March 1968

Contract No. NAS5-10307

Prepared by

H. G. Carlson
G. A. Brown
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D. L. Dugger
R. J. Proebsting

Texas Instruments Incorporated
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Dallas, Texas 75222

for

Goddard Space Flight Center
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TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

TABLE OF CONTENTS (Continued)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

LIST OF ILLUSTRATIONS (Continued)

LIST OF ILLUSTRATIONS (Continued)

LIST OF ILLUSTRATIONS (Continued)

LIST OF ILLUSTRATIONS (Continued)

LIST OF TABLES

LIST OF TABLES (Continued)

SECTION I

INTRODUCTION

The purpose of this contract was to investigate the properties of dielectric materials which could be applied to silicon monolithic metal-insulator-silicon (MIS) field effect transistor (FET) circuits. It was also a requirement to develop a thin film, high sheet resistance, resistor technology compatible with monolithic device integrated circuit technology. The program was instituted in particular to develop technologies which could result in improved stability of MISFET circuits in a space radiation plenum.

Early discussions between R. W. Warner* of Texas Instruments and NASA officials had intended a cursory investigation of a wide variety of dielectric materials deposited by chemical reaction as well as rf sputtering from a stoichiometric anode. However, preliminary work with silicon nitride deposited by reaction of silane and ammonia in a hydrogen diluent yielded reduced MISFET turn on voltage and improved radiation tolerance. Hence, the decision was made by T. Sciacca and J. L. Tarpley of National Aeronautics and Space Administration and H. G. Carlson of Texas Instruments to pursue the development of silicon nitride MISFET technology and compatible cermet resistors to yield an integrated circuit including MISFETS with threshold voltages of less than two volts and resistor elements from 10^5 to 10^6 ohms. The reduction to practice of such technology was thought to be more important to NASA at that time than further cursory investigation of new dielectric materials. A circuit designed by NASA was furnished as the model for technology demonstration of the silicon nitride and cermet resistors. The NASA circuit was of the conventional silicon dioxide gate dielectric form and utilized load resistors external to the individual circuit packages.

The majority of this report is concerned with the development of the MNOSFET (N = silicon nitride, 0 - silicon dioxide) transistor technology and a simple cermet

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*Now director Semiconductor Research Development Laboratories, ITT, Miami, Florida

resistor process. At the request of NASA, a rather lengthy comparison of the cermet resistor technology is made with other resistor formation techniques for monolithic resistor elements. This should be skipped by readers familiar with the field. While the techniques for formation of silicon nitride are applicable to a wide variety of integrated circuits, the simple evaporation technique for cermet resistors is not believed to be suitable for production applications. However, the evaporation procedure is sufficiently described so that small scale application of the technique can be made by readers with reasonable yields.

SECTION II

DEVELOPMENT & CHARACTERISTICS OF METAL-NITRIDE-OXIDE-SILICON INSULATED GATE FIELD EFFECT TRANSISTORS

A. PREPARATION AND PROPERTIES OF SILICON NITRIDE

A great amount of interest has developed during the last three years in silicon nitride as a material for the passivation and stabilization of semiconductor devices. This has resulted largely from the realization that silicon nitride serves as a barrier to the migration of charged ionic species, a major source of device instability.

In addition, silicon nitride has a dielectric constant approximately twice that of silicon dioxide, very high dielectric strength, and can be prepared in such a way that pinhole densities are very low. These properties suggest that silicon nitride might well be applied in the formation of gate insulators for insulated gate field effect transistors and integrated circuits. This section of the report is concerned with the development of such structures at Texas Instruments, and the fabrication and characterization of the metal-silicon nitride silicon oxide field effect transistors (MNOSFET's) included in the binary counter circuits delivered to NASA.

The preparation of silicon nitride films in a form suitable for device applications was first reported by Sterling and Swann[1] and Doo, Nichols and Silvey.[2] So much interest was generated that a symposium devoted completely to silicon nitride was held.[3]

The silicon nitride films for device applications at Texas Instruments are prepared by reaction of silane and ammonia in hydrogen diluent at 850°C.

The preparation and physical properties of these films have been described in detail by Bean, Gleim, Yeakley, and Runyan;[4] Brown, Robinette, and Carlson[5] have studied the electrical characteristics and their dependence upon fabrication parameters. Figure 1 summarizes the most important results of these investigations from the standpoint of device applications. The dependence of the deposition rate, etch rate, index of refraction, high field resistivity, and dielectric constant upon silane-ammonia ratio is given for the films formed at 850°C. It is seen from these results that in

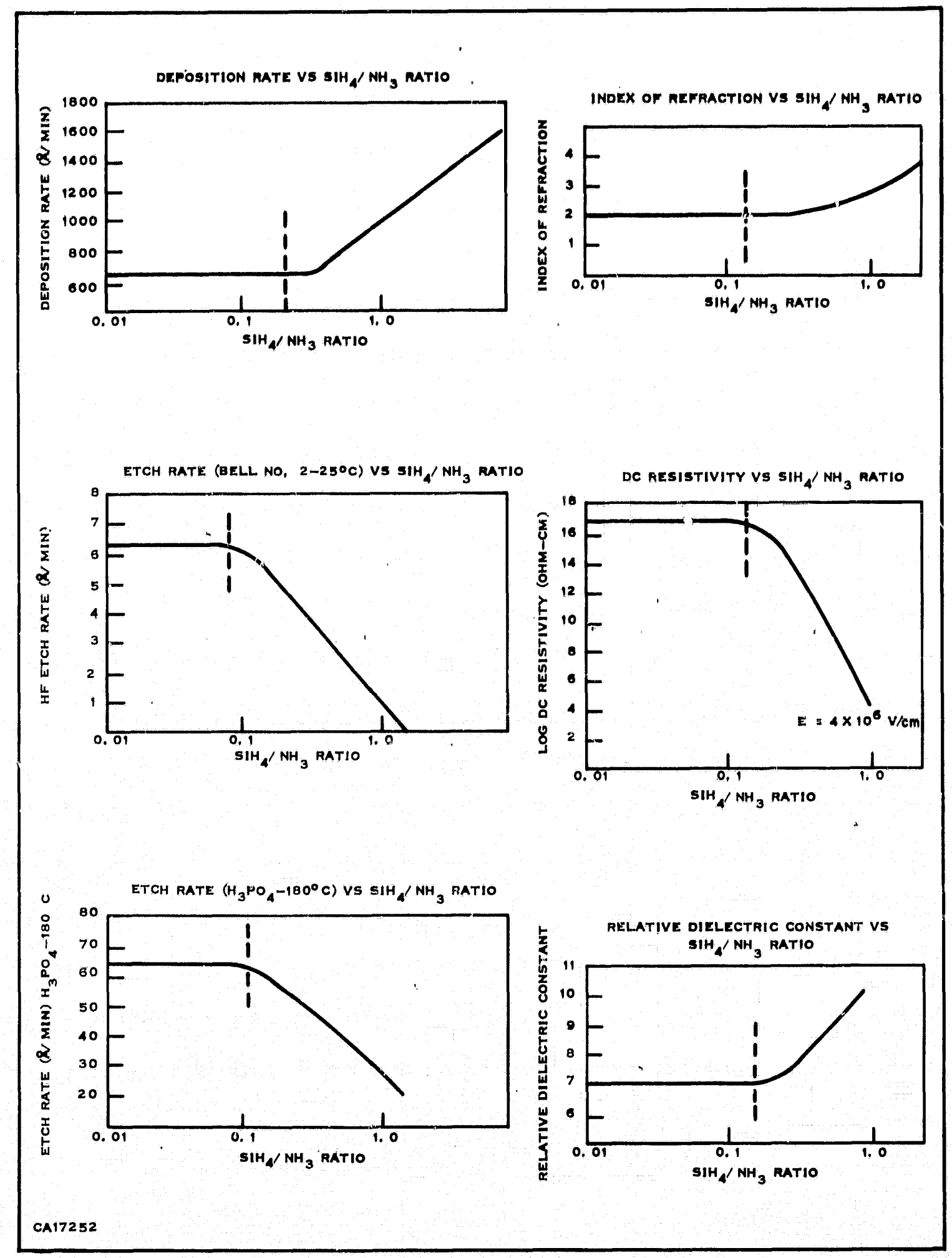


Figure 1. Properties of Silicon Nitride

general films with the most desirable characteristics are formed at silane-ammonia ratios below 0.1. The constancy of all the characteristics in this low-silane regime is an aid in the establishment of a stable, reproducible process.

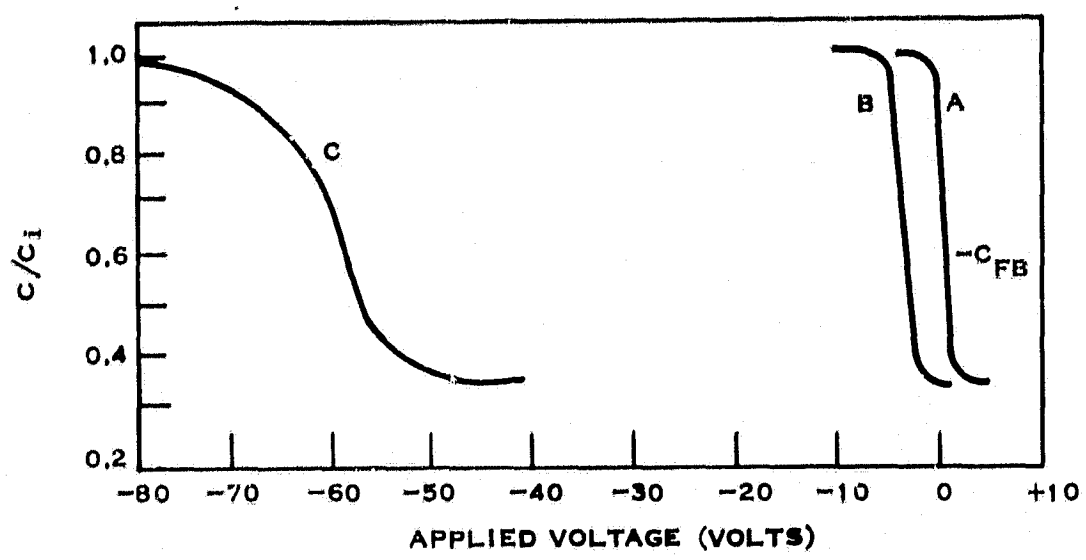
B. CHARACTERISTICS OF THE MNS AND MNOS SYSTEMS

When given the deposition and etching technologies, and the diffusant masking properties of silicon nitride films reported in the literature, [1-4, 6, 7] the question naturally arises whether silicon nitride might completely replace silicon dioxide as a passivating element in silicon-planar-device technology. The experiments described below indicate that, at least in most applications, this complete replacement will not result in the most desirable device characteristics.

Figure 2 compares the capacitance-voltage characteristics of various metal-insulator-semiconductor capacitor structures having the same insulator capacitance per unit area with the C-V characteristic of an idealized MIS capacitor having the same parameters. Curve A is computed for the idealized structure, assuming no metal-semiconductor work function difference, no surface states and no charge in the insulator. Curve B was obtained experimentally on samples formed either by thermal oxidation to a thickness of 1500 Å and annealing, or by thermal oxidation to 1000 Å and subsequent depositions of a 900 Å layer of silicon nitride. Curve C was observed experimentally when the silicon surface was vapor etched and 2750Å of Si_3N_4 deposited in situ to avoid any SiO_2 layer under the Si_3N_4 on the silicon surface.

The high, negative flat-band voltage of Curve C is indicative of a large amount of positive charge associated with the nitride-silicon interface. Such a condition would cause severe inversion of P-type surface regions on transistors or integrated circuits. The smeared-out nature of the C-V relationship is evidence of a high density of chargeable interface states at the nitride-silicon interface. These states can act as traps or recombination centers for carriers being transported in the vicinity of the surface. Such action can result in poor junction characteristics and low device gain.

In contrast, the characteristics of the equivalent MOS and MNOS devices are indistinguishable on the scale shown (Curve B). This indicates that the beneficial characteristics of the thermally-grown oxide-silicon interface can be coupled with the contamination-shielding properties of silicon nitride through the use of an MNOS system. Very thin oxide layers are sufficient to ameliorate the interfacial characteristics



CURVE	INSULATOR MATERIALS (THICKNESS)	FLAT BAND VOLTAGE
A	IDEALIZED; $C_i = 2.3 \times 10^{-8}$ fd/cm^2	0
B	SILICON DIOXIDE (1500 Å); OR SILICON DIOXIDE (1000 Å) + SILICON NITRIDE (900 Å)	-4
C	SILICON NITRIDE (2750 Å) ON VAPOR-ETCHED SILICON	-61

SUBSTRATE: P-TYPE SILICON, $N_D = 10^{15}$/cm^3

CA14900

Figure 2. MIS Capacitance-Voltage Characteristics of Structures with Equivalent Specific Capacitance

indicated by Curve C. Even the native oxide normally found on silicon slices (20 to 50 Å in thickness) greatly improves the C-V characteristics, yielding curves intermediate between B and C.

Evidence of electronic-charge instabilities[8] in the nitride-silicon interface is given in Figure 3 which shows C-V curves drawn for MNS capacitors by an automatic curve tracer with a voltage sweep rate of 0.3 V/sec. The large amount of hysteresis and its polarity are suggestive of electronic-charge injection by tunneling across the nitride-silicon interface and subsequent selective trapping in the nitride; this

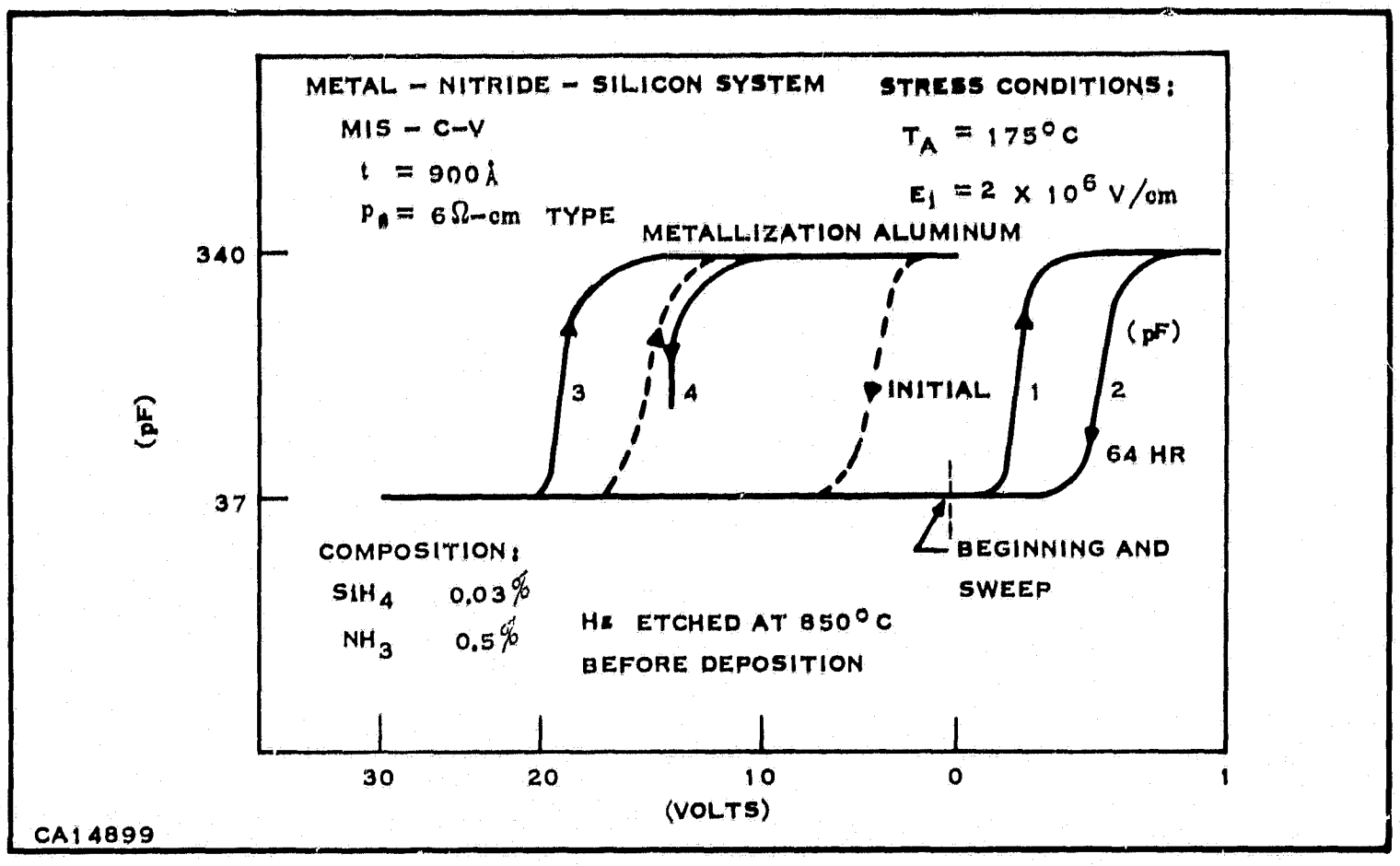


Figure 3. Metal-Nitride-Silicon Capacitance-Voltage and Stress Characteristics

temporarily changes the electrical potential near the interface. The instability under 300°C, 2 x 10^6 V/cm stress conditions is of a polarity opposite to that predicted by a model based upon drift of ions contained in the insulator, but is consistent with the electronic charge interaction described above. In this regard, the oxide in the MNOS structure can be thought of as a barrier to electrons attempting to tunnel from the silicon into allowed levels in the silicon nitride.

With the above considerations in mind, the design of a suitable MNOS gate insulator structure may be undertaken. The desire for p-channel enhancement mode transistors of low threshold voltage suggests the use of (100) oriented n-type silicon substrates. From the point of view of minimizing threshold voltage and increasing speed, it is desirable to maximize the specific capacitance of the insulator structure, either by increasing the average dielectric constant or by decreasing the thickness. The onset of the tunneling-slow trapping mechanism discussed above sets a lower limit on the oxide thickness, and hence, insulator thickness that will produce desirable devices. For most structures, an oxide thickness of approximately 200Å might be regarded as a safe lower limit to ensure suppression of this mechanism.

The relationship between speed and specific capacitance comes about because of the stray capacitances associated with the circuit, since in an ideal IGFET, speed is independent of insulator capacitance. This is because switching speed is proportional to the ratio of transconductance to input capacitance, and in the ideal case, both these parameters depend linearly upon the specific capacitance of the gate. If a fixed stray capacitance is associated with the device, however, increasing the gate capacitance increases the transconductance proportionally more than the overall input capacitance, and circuit speed increases.

For these reasons it was decided tc develop a gate insulator having a specific capacitance equivalent to 500Å of SiO_2 (6.8×10^{-8} fd/cm^2). It is difficult to form reliable oxide capacitors of this thickness because of high pinhole densities and low breakdown voltages. It was decided somewhat arbitrarily to locate the oxide-nitride interface in the electrical center of the insulator structure; that is, both oxide and nitride films having a specific capacitance of 1.36×10^{-7} fd/cm^2. This yields an oxide thickness of 250Å, great enough to resist tunneling instability for reasonable applied voltages; and a silicon nitride thickness of 460Å, using the relative dielectric constant of 7 shown in Figure 1. Thus the total gate insulator is designed to be 710Å thick; since it is made up of two layers, one thermally grown and the other deposited, it may be expected to have a low pinhole density.

Before undertaking the fabrication of two-layer dielectric structures, studies on the fabrication and characteristics of very thin silicon dioxide and silicon nitride films were carried out separately, using ellipsometry and MIS capacitance-voltage techniques. Some of the results of these studies are shown in Figure 4. Here is plotted the measured flat-band voltage of various MIS capacitors as a function of their effective thickness. This effective thickness is defined by the relation

$$W'_{ox} = W_{ox} + \frac{\epsilon_{ox}}{\epsilon_n} W_n$$

For SiO_2 films the second term or the right is of course zero and $W'_{ox} = W_{ox}$. For oxide-nitride films, W'_{ox} is seen to be the thickness of an SiO_2 layer having the same specific capacitance as the bi-layer film in question.

The source of a plot of the type shown in Figure 4 is the equation

$$V_{fb} = \phi - \frac{Q_{ss}}{\epsilon_{ox}} W'_{ox}$$

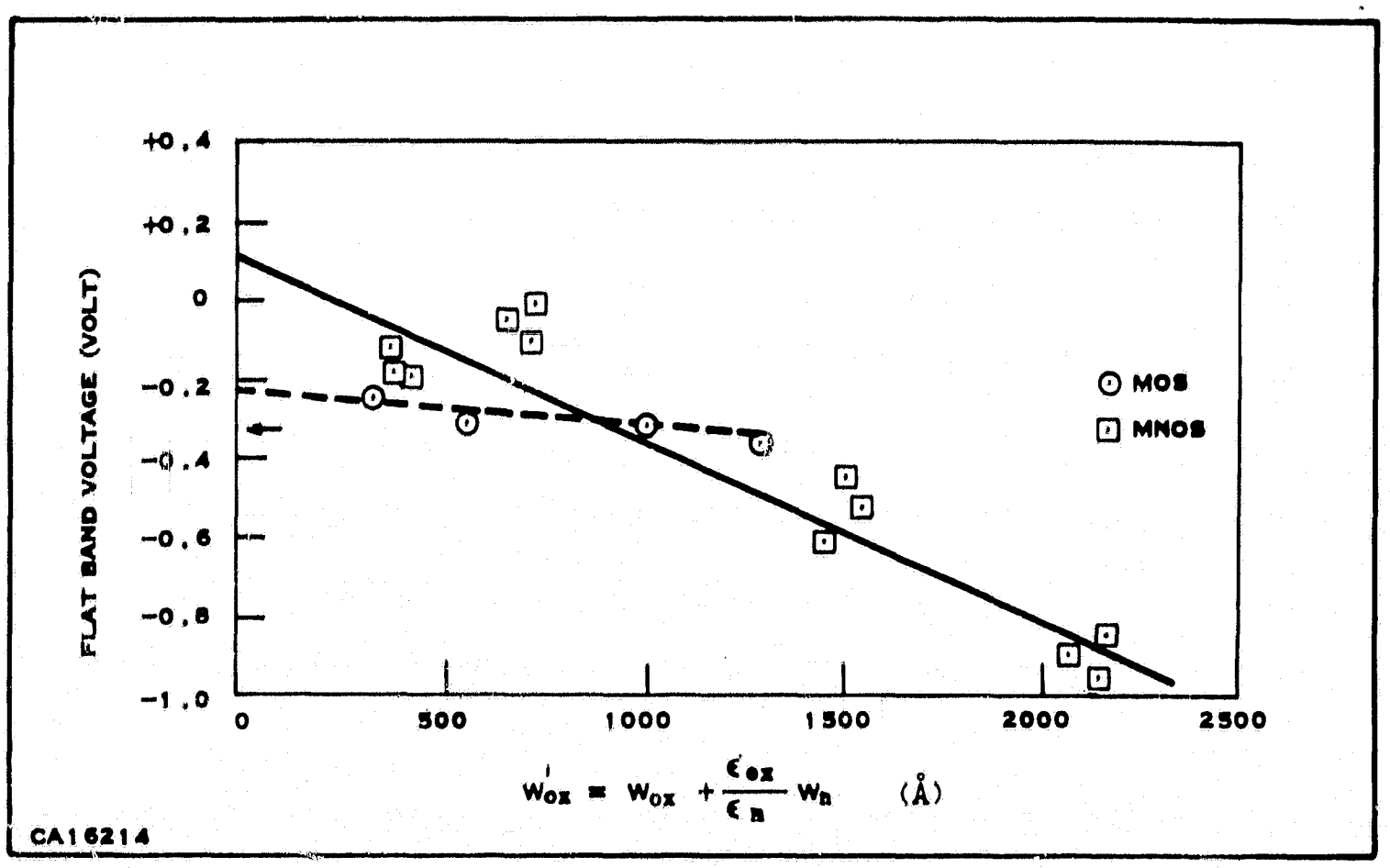


Figure 4. Aluminum, Silicon Dioxide, Silicon and Aluminum, Silicon Nitride, Silicon Dioxide, Silicon Systems

which describes the effect on the flat-band voltage of an MIS capacitor the total work function difference throughout the system, ϕ; and the weighted sum of surface state and bulk insulator charge (including charge associated with any insulator-insulator interface), Q_{ss}. The ordinate intercept of such a plot yields ϕ, while Q_{ss} is obtained from the slope of the curve.

The open dots and dashed line of Figure 4 represent a series of experiments performed with thin SiO_2 layers grown on (100) oriented n-type silicon doped to $3\text{-}4 \times 10^{14}$ atoms/cm^3. This is the same material used in the fabrication of the IGFET's to be described below. Aluminum contacts evaporated via an electron beam technique were used in all experiments. The preparation cycle was as follows:

1. Vapor etch the silicon surface in H_2 - HCl vapor at 1250°C removing approximately 10 microns of silicon.
2. Oxidize at 1100°C in dry O_2 (liquid source) to the desired thickness-bake in dry N_2 at 1100°C - 20 min.
3. Evaporate aluminum — define contact pattern photolithographically.
4. Anneal oxides at 500°C in dry N_2 for 20 min. or until C-V characteristics stabilize.

Capacitance voltage curves were measured at 1 MHz using an automatic plotter. The flat-band capacitance was computed for each curve from computer calculation of ideal high frequency C-V characteristics and detailed fitting of the experimental curves.

The slope of the dashed line of Figure 4 yields a Q_{ss} of $2 \times 10^{10}/cm^2$. It is of interest to note that the intercept value, ϕ, is approximately 100 millivolts lower than that quoted for the Al - SiO_2 - Si ($3 \times 10^{14}/cm^3$) system by Deal, et al.[9] This discrepancy, while small, is sufficient that negative or zero values of Q_{ss} would have been inferred from measurements of any single capacitor up to approximately 1000Å in thickness.

The two-layer structures were formed by a process identical to that described above up to the completion of oxidation. Then after the dry nitrogen flush, hydrogen was turned on and the reactor temperature lowered to 850°C for silicon nitride deposition. In all cases, oxide-nitride layers are formed in a single reactor operation, and the relationship between oxide and nitride thickness in any run is

$$W_{ox} = \frac{\epsilon_{ox}}{\epsilon_n} W_n.$$

After deposition, the oxide-nitride structures are processed exactly like the oxides described above. The only difference in process is that often it is necessary to anneal the electron beam evaporated capacitors for as much as one hour at 550° C in N_2 to stabilize the C-V characteristic.

The greater slope of the solid curve of Figure 4, representing the MNOS structure, indicates either that the presence of the nitride inhibited the annealing process or that more charge is present somewhere in the structure. The slope shown corresponds to $Q_{ss} = 1 \times 10^{11}/cm^2$. The ordinate intercept, ϕ, is shifted positive about 0.4 volts from that observed with the oxide alone. This effect is in the same direction as that reported by Nigh, et al[10] for the Al_2O_3-SiO_2-Si system.

C. MNOSFET CONSTRUCTION

The work of MNOS capacitors described above indicated that silicon nitride on thermal oxide should make an ideal gate dielectric for an insulated-gate field-effect transistor.

Two processes for the formation of MNOSFET transistors are currently being employed by Texas Instruments. The first is illustrated in Figure 5. In this

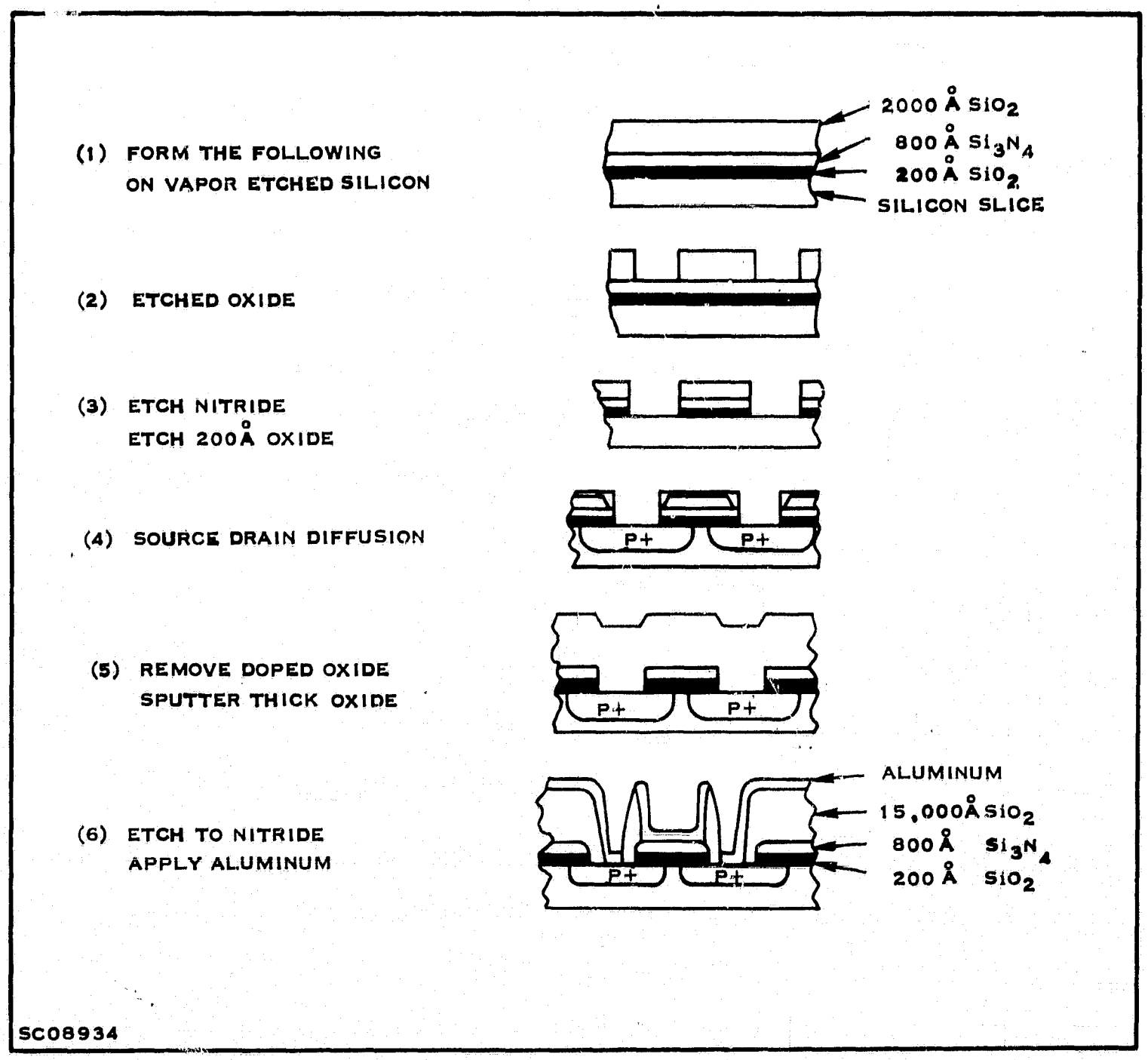


Figure 5. Silicon Nitride Process for MNOS Transistor Fabrication

case the silicon surface is first vapor etched in 5% HCl in H_2 and oxidized without removal from the vapor-etched system, utilizing techniques previously demonstrated to produce stable clean oxide MOSFETs.[11] Silicon nitride is then deposited over the oxide before the wafers are removed from the reactor. A film of silicon oxide is then deposited over the silicon nitride by a silane and oxygen reaction at 400°C. The source drain diffusion apertures are then formed using the 180°C H_3PO_4 etching procedure of Van Gelder and Hauser.[12] Deposition and diffusion of the source-drain junctions, accompanied by oxidation of the diffused surface follows. Contact apertures can then be formed by standard techniques, and the evaporation and definition of the metal pattern completes the process. A thick oxide may be applied and selectively removed as shown in the illustration to lower stray capacitance, if desired.

The second process, which was used in the binary counter for NASA discussed in Section IV, involves deposition of the nitride film near the end, rather than at the beginning of fabrication. In this sequence, outlined in Figure 6, standard techniques are employed in planar oxidation and definition of source-drain diffusion areas. Deposition followed by diffusion of the source drain regions is carried out to a point just short of the desired final junction depth. All oxide is then removed from the channel regions using photoresist techniques. The slices are then transferred to a reactor where the silicon dioxide-silicon nitride structure is formed in a single step as above, and the junction diffusion is completed. Silicon dioxide is then deposited as a silicon nitride etch mask and the contract apertures are etched. A metallization sequence completes the process. Experimentation has revealed advantages and disadvantages in both processes. The first process results in an inherently more stable structure because of the sealing of the surface early in the process by the silicon nitride deposition. In the form described, it suffers from a silicon nitride-silicon oxide abutment under the gate metallization which can be the site of gate short circuits. The second process is more sensitive to contamination in processing, but the finished device is protected by a smooth coat of silicon nitride over everything except the contacts.

MNOS insulated-gate field-effect transistors and Integrated Circuits have been built in a variety of configurations. Figure 7 shows the pattern used for exploratory studies. The device in the lower left-hand corner of the 100-mil square chip comprises two MIS transistors, one a surrounded-drain depletion mode type unit and the other a standard bar-type enhancement mode type device. Source-drain window spacing is 0.4 mil. Directly above this pattern is a large transistor structure with a 20-mil square channel. This is useful for studies of low field inversion layer-charge transport effects, and furnishes a transistor upon which meaningful gate-to-substrate capacitance-voltage characteristics are measurable.

The device in the upper right-hand corner of the chip is an MIS capacitor with guard ring formed exactly as the gate regions of the transistors. Below the capacitor is a PN junction formed exactly as the source-drain junctions for analysis of diode characteristics.

Figure 8 shows the MNOSFET binary-counter circuit with cermet thin-film load resistors built under this contract. The P-channel transistors comprising the circuit are in the lower left-hand part of the chip, while a pattern of four discrete transistors of differing gate width is in the lower right-hand corner.

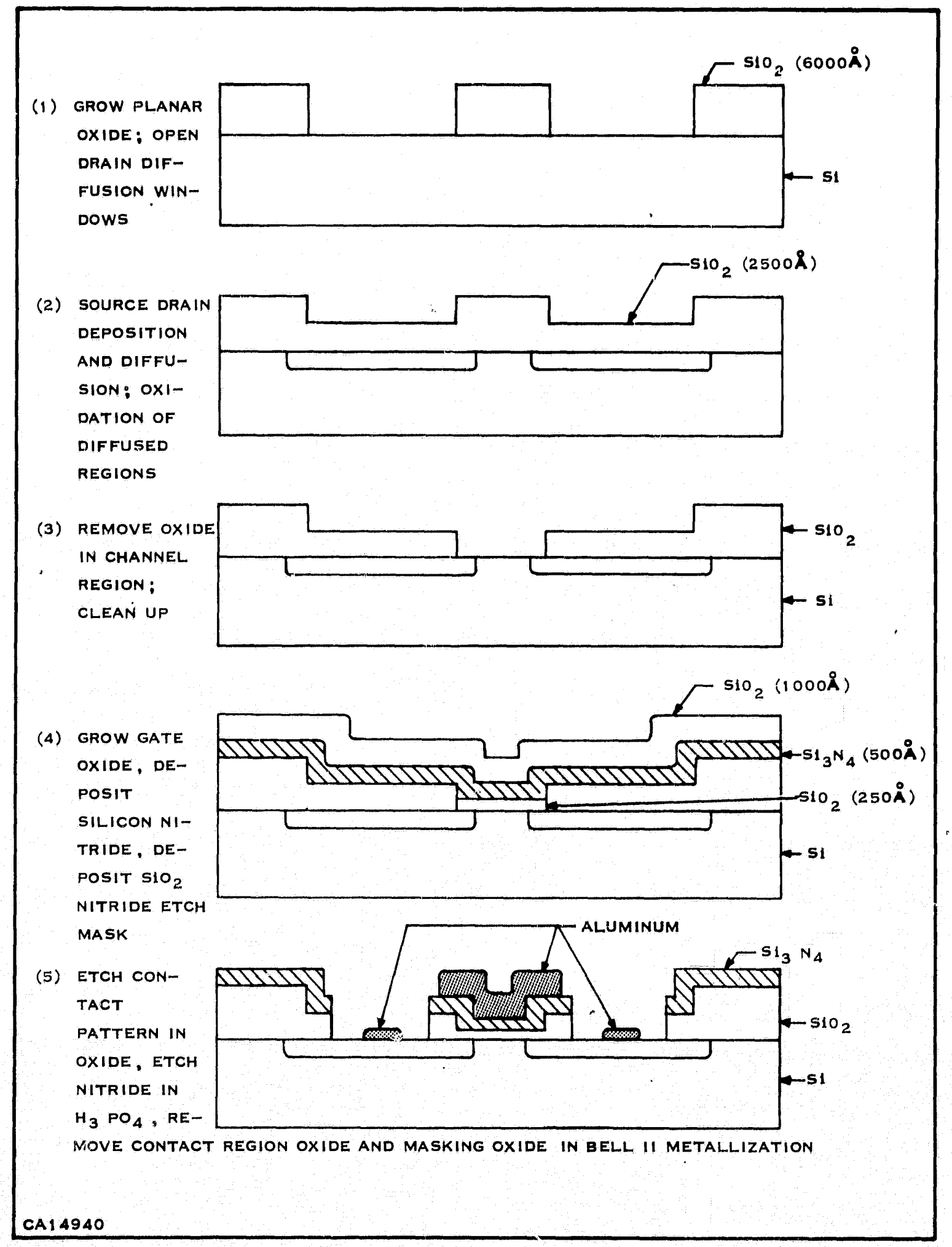


Figure 6. Second Process for Fabricating MNOS Field-Effect Transistors

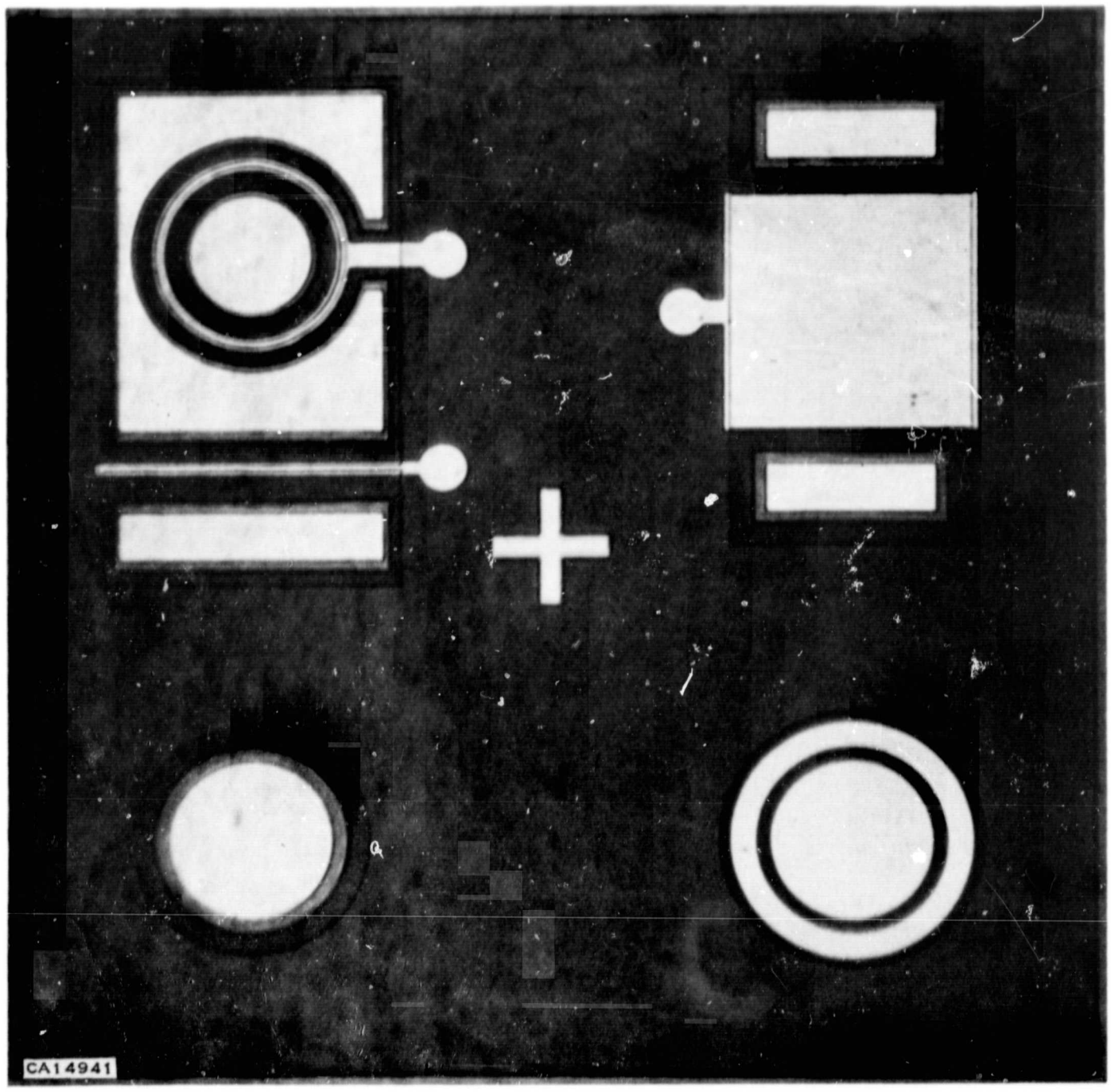


Figure 7. Exploratory MISFET Configuration

The gate insulator on these circuits is 250 Å SiO_2, 470 Å of Si_3N_4 and has a specific capacitance equivalent to 500Å of silicon dioxide, fabricated by the techniques techniques described above.

D. CHARACTERISTICS AND STABILITY OF MNOSFET'S

In this section of the report, the electrical characteristics of various MNOSFET's, including some units from the material group from which devices were supplied to NASA, will be evaluated. Major emphasis will be placed upon the initial

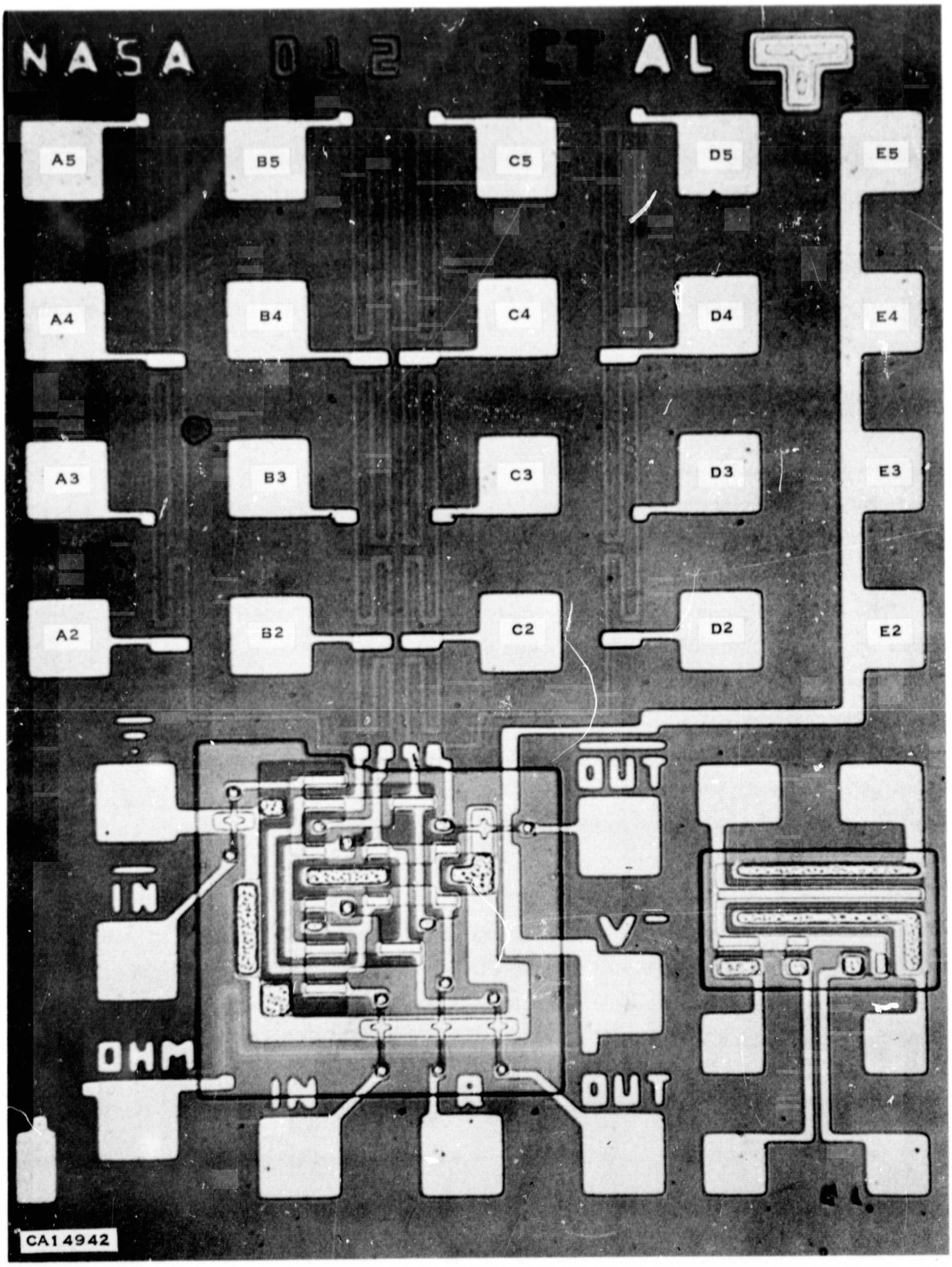


Figure 8. MNOSFET Binary Counter Circuit

threshold voltage (V_t) of the devices and the stability of this V_t value under thermal-electrical stress conditions which will include the T_A=175°C, $E_{ox} = \pm 2 \times 10^6$ volt/cm, 168 hour test condition requested by NASA.

For this type of study it is desirable to employ measurement techniques which will result in threshold voltage values which are meaningful in terms of the physics of the device structure. Analyses of the current-voltage characteristics of insulated gate field effect transistors [13, 14] have shown that a threshold voltage is most easily defined and related to device parameters when the transistor is operated in the resistive, or triode regime with $V_d \approx 0$. In this regime, the drain conductance,

$$g_d = \frac{\partial I_d}{\partial V_d}\bigg|_{V_g}$$

increases linearly with V_g for small values of g_d. The threshold voltage is thus defined as the voltage-axis intercept of the g_d -V_g plot extrapolated from the linear regime. This definition serves as the basis for the measurements made in this study. A test set for the measurement of g_d -V_g characteristics is shown in Figure 9. Here a constant voltage source ($R_{in} \simeq 10\ \Omega$) maintains a drain voltage of 100 mvdc. In series with the IGFET channel is a current-measuring resistor R_c which is varied in value from 10 to 1000 ohms depending upon the characteristics of transistor to be measured. The conductance of this resistor is chosen to be two orders of magnitude larger than the largest value of transistor conductance to be measured. It will be noted that the arrangement of circuit elements causes the voltage developed across this current-measuring resistor to appear as part of the gate-source potential. This was done to facilitate grounding of the circuit components, and since the resistor voltage never exceeds 1 mv, its effect can be ignored. The gate potential is swept over the region of interest using a Hewlett-Packard 202A Low Frequency Function Generator as a triangular wave generator (rep. rate = 0.008/sec) in conjunction with a dc voltage supply. The gate voltage source is connected to the horizontal terminals of an X-Y recorder which acts as a voltmeter while the voltage across the current measuring resistor is connected to the vertical terminals. The drain conductance, assuming a resistive channel, is given by

$$g_d = \frac{I_d}{V_c} = \frac{V_c}{R_c\ V_d}$$

where V_d is the voltage developed across the current measuring resistor R_c (known) and V_d is the drain voltage (100 mv).

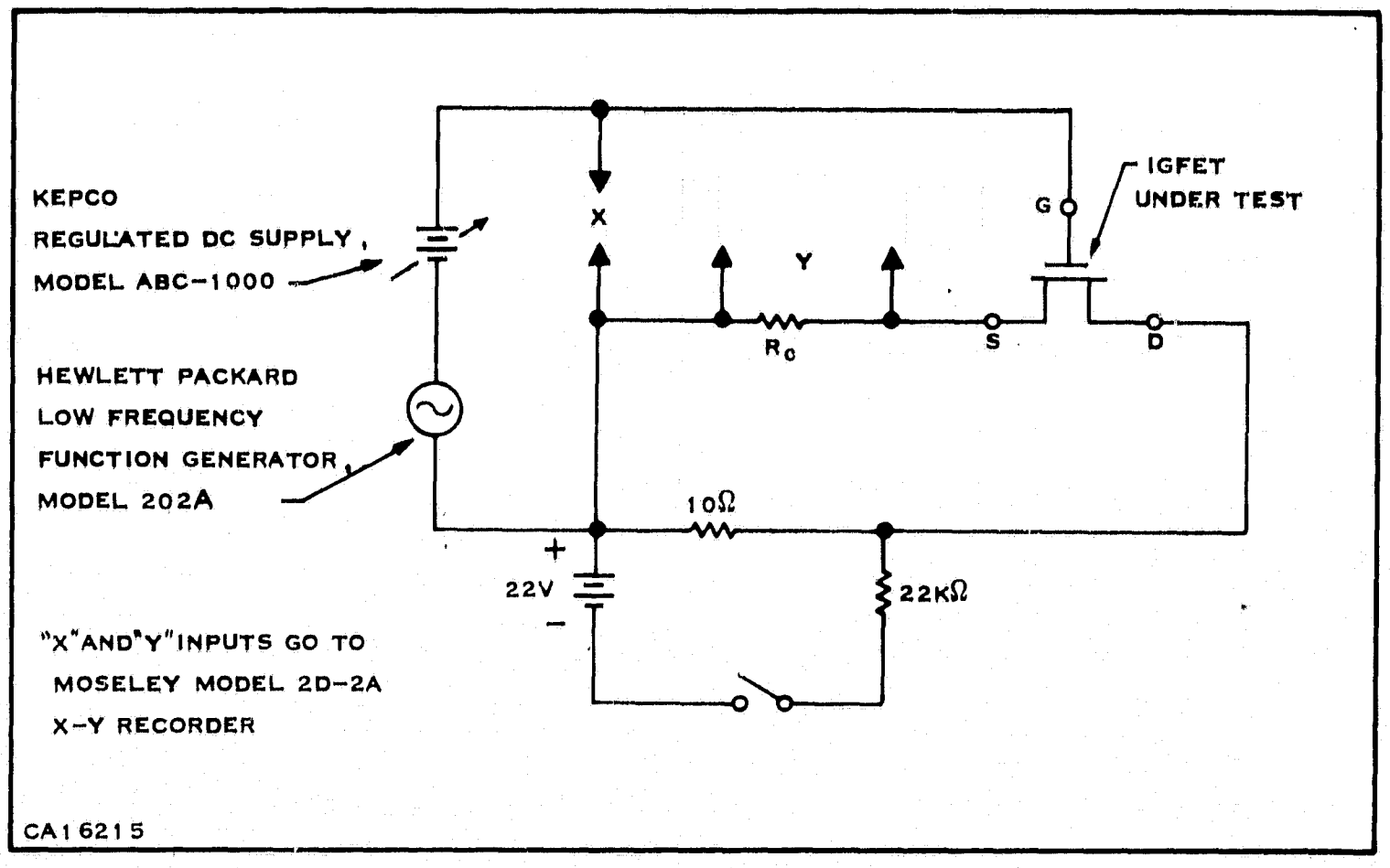


Figure 9. Circuit Schematic for Generating g_d versus V_g Characteristic for an Insulated Gate Field-Effect Transistor

An example of the plots obtained from the test set is given in Figure 10 where the g_d versus V_d curves of all four discrete transistors in the test pattern shown in Figure 9 are presented. A threshold voltage of -1.5 volts is observed. These measurements were made on a chip from the material group which was used to supply Integrated Circuits* to NASA. The convex-upward curvature of the g_d versus V_d characteristics may be interpreted in terms of a high field mobility decrease of the carriers [15] or parasitic resistance associated with the electrical contacts to the channel.

The different slopes of the curves near the abscissa intercept reflect the different channel widths of the devices in the pattern. Nominal channel widths are as follows:

Drain #	Nominal Channel Width (mils)
1	2
2	1

*Trademark

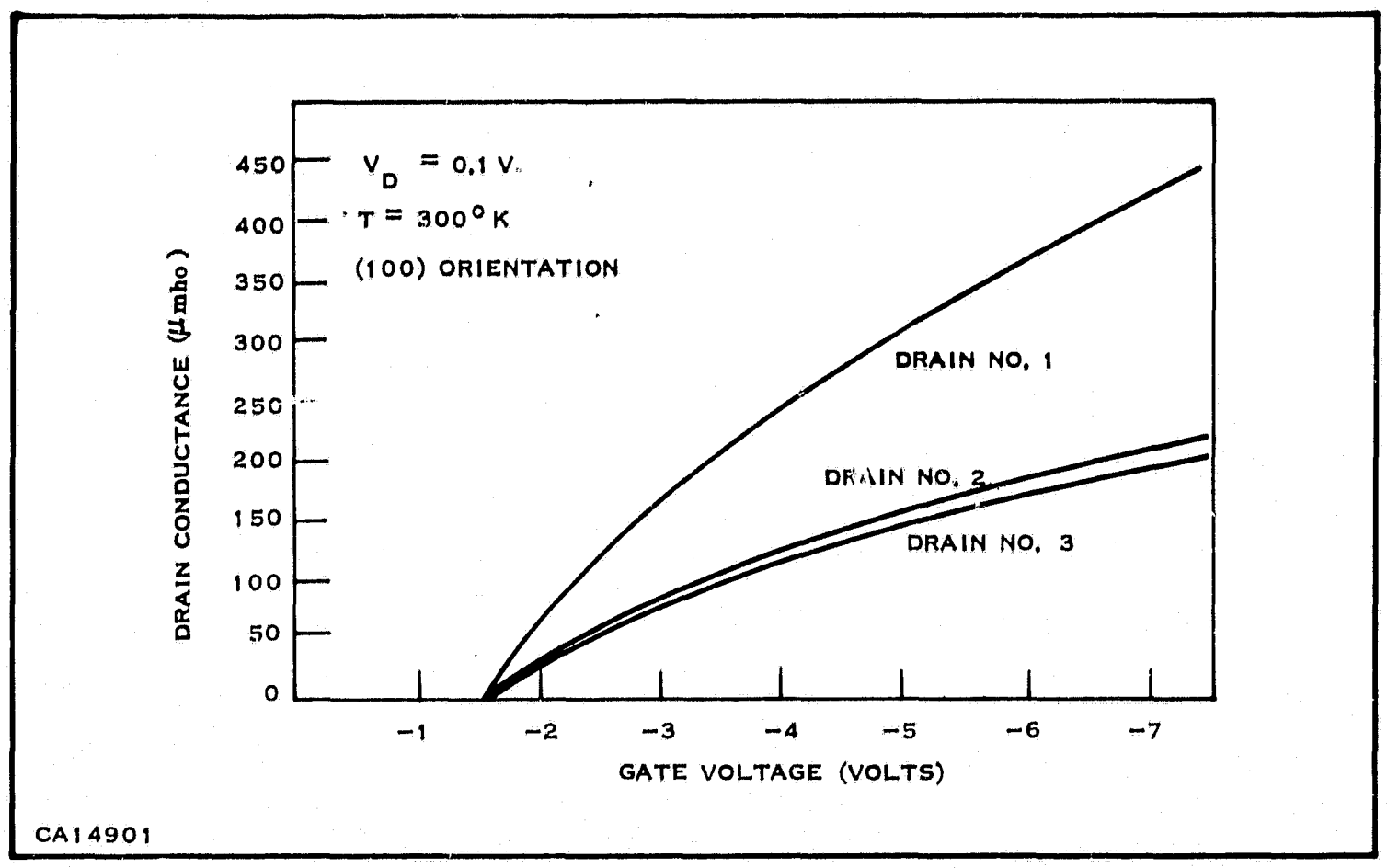


Figure 10. MNOSFET Drain Conductance versus Gate Voltage

Drain #	Nominal Channel Width (mils)
3	1
5	10

The channel length of all the units is estimated to be about 0.3 mils.

The procedure for stress-testing these devices begins with the mounting of chips in 6-pin TO-5 headers and gold-ball-bonding leads to the discrete transistor pattern as shown in Figure 9. The units are then sealed in a dry nitrogen atmosphere.

The voltage that must be applied to the gate electrode relative to the source-drain-substrate to achieve a given electric field strength in the oxide portion of the gate insulator is computed under the assumption that the electric displacement vector is continuous through the insulator, that is

$$D_i = \epsilon_{ox} E_{ox} = \epsilon_n E_n$$

where

D_i = electric displacement vector in insulators

ϵ_{ox}, ϵ_n = dielectric constant of oxide, nitride

E_{ox}, E_n = electric field strength in oxide, nitride.

The total insulator voltage for a given oxide field strength is then obtained by integration, giving

$$V_{stress} = (W_{ox} + \frac{\epsilon_{ox}}{\epsilon_n} W_n) E_{ox}$$

If the exact thicknesses of the oxide and nitride films are not known, an equivalent determination can be made from the measurement of the insulator capacitance, C_i, using a metal electrode of area A, the relation being

$$V_{stress} = \frac{\epsilon_{ox} A}{C_i} E_{ox}$$

Devices are initially measured on the g_d-V_g test set, then are mounted in a test board and the proper magnitude and polarity of stress voltage is applied. They are then placed in an oven at the desired ambient temperature for the required test period, then removed and cooled to room temperature with bias applied. After they are cooled, they are removed from bias and remeasured. Extrapolated values of V_t are recorded at each checkpoint.

An example of the results of such testing is shown in Figure 11 for a P-channel MNOSFET having a gate insulator equivalent to 1000Å of SiO_2, fabricated on (111) oriented silicon. These devices were built before the NASA circuit work was begun. The initial threshold voltage value was -3.7 volts. Stress testing with T_A = 300°C and a gate voltage of -10 volts (E_{ox} = 1 x 10^6 volt/cm) revealed that under positive gate bias, the device exhibited a 0.2 volt V_t instability of a polarity attributable to ionic drift in the oxide, and that under negative gate bias, the threshold voltage returned to its initial value. This device failed between the 6 hour and 10 hour checkpoints because of purple plague formation on the source-drain contacts. Stress testing on other devices from this group at T_A = 175°C have extended to a total of 233 hours with the same or less instability than that described above.

Two series of tests were performed on devices from the group which yielded the circuits supplied to NASA. Unfortunately these units were among the least stable MNOSFET's that have been tested.

In the first test sequence, two test patterns of four transistors each were stressed at 175°C with a gate voltage of 10 volts, which corresponds to an electric field strength of 2 x 10^6 volt/cm in the 250Å oxide layer. Positive gate bias was

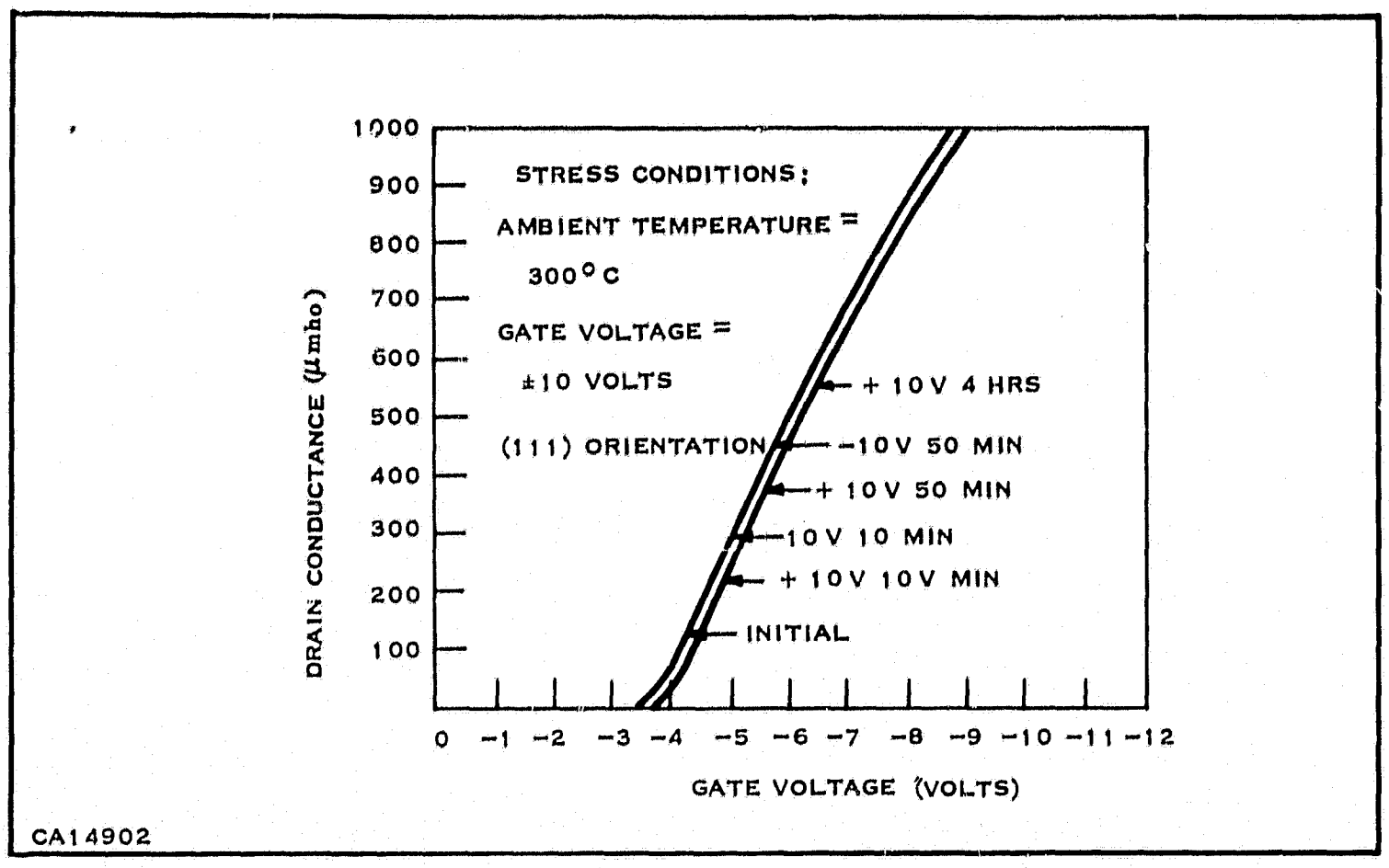


Figure 11. Discrete MNOSFET Drain Conductance versus Gate Voltage

maintained for the first 110 hours of the test, with V_t checkpoints after a total of 1, 9, 18, and 110 hours. At this point the polarity of the gate stress was reversed and V_t was checked after 1, 17, and 58 hours. The quantity $\Delta V_t = V_t$ (checkpoint) $-V_t$ (initial) is plotted versus stress time in Figure 12 for one device from each chip. All devices on on a given chip display the same voltage shifts within experimental error.

The device from the first chip, which had an initial threshold voltage of -1.7 volt, displayed readily explainable if not completely desirable instability characteristics. After one hour of positive gate bias stress, the threshold had shifted about 0.6 volt negative, the polarity expected from the mechanism of ion migration within the oxide. The 9, 18, and 110 hour checkpoints established the saturation of this effect at this stress level at a ΔV_t of approximately -0.7 volt. Polarity reversal of the voltage stress returned the V_t value to within 0.2 volt of its initial value within one hour, and the value was maintained at less than 0.1 volt until termination of the 168 hour test period.

The second chip (V_t (initial) = -1.52 volt) under this test cycle displayed the same pattern except for an anomalous 0.9 volt positive threshold voltage shift under positive bias between the one and nine hour checkpoints. The polarity of this

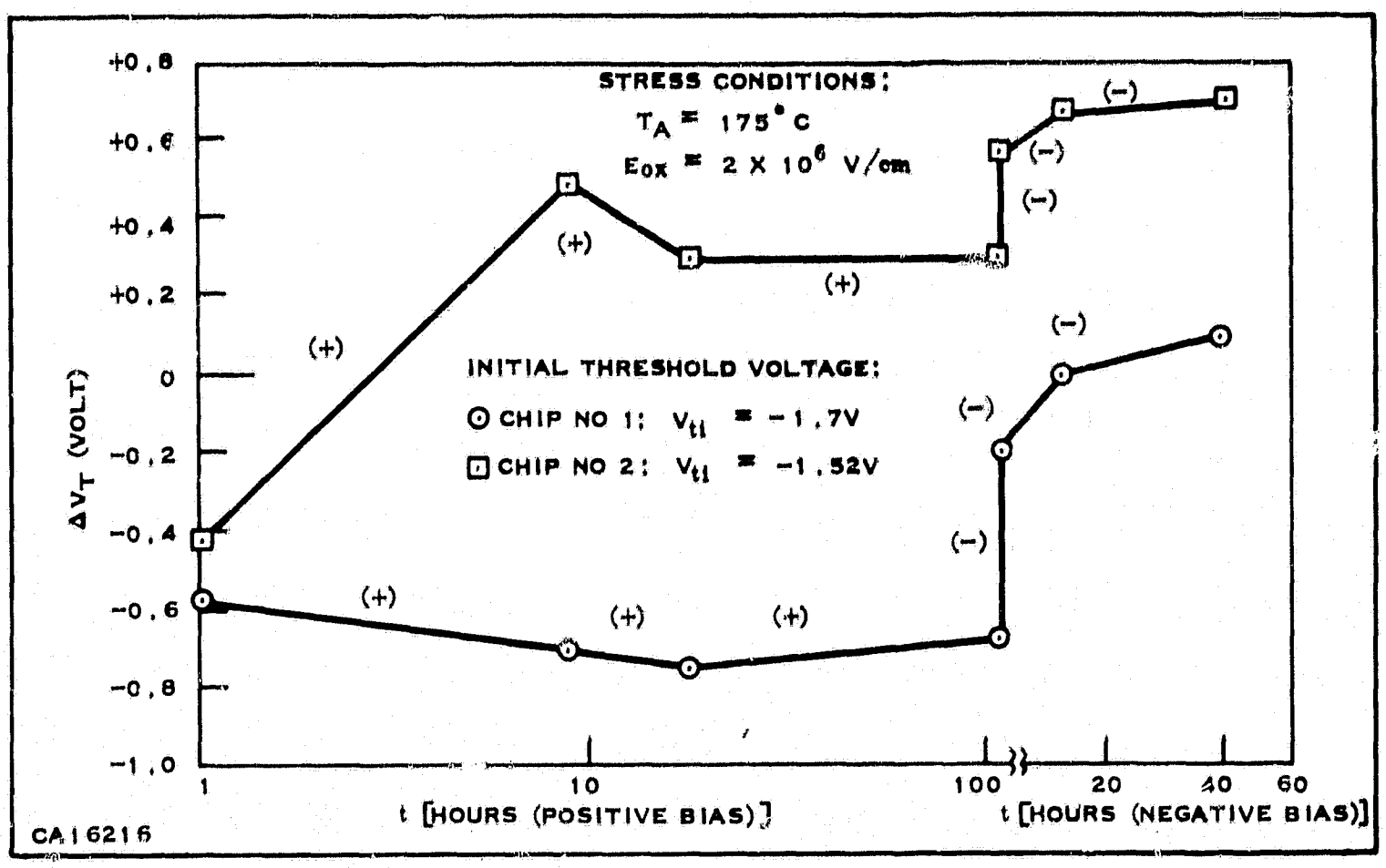


Figure 12. NASA Circuit Transistor Threshold Voltage Stability, Test Cycle No. 1

shift is that expected for the tunneling — slow trapping mechanism discussed in the previous section. However in this structure a pulse amplitude of the order of 50 volts would probably be required to induce such a shift, and there is little reason to think that this device was exposed to such a stress.

The second test cycle under the 175°C - 2 x 10^6 volt/cm stress condition consisted of alternating positive and negative gate polarity for stress times as follows: 1/2 hour (+), 1/2 hour (-), 16 hours (+), 16 hours (-), 68 hours (+), 68 hours (-). The results of this test are shown graphically in Figure 13. The first chip, which displayed an initial V_t of -1.45 volt, exhibited a 1.1 volt instability of the tunneling-slow trapping polarity during the first half hour of stress, but all further shifts were of the opposite or ionic-drift type polarity. The other chip, having V_t (initial) = -1.0 volt showed no dominance of tunneling-slow trapping instability at any checkpoint, maintaining $|\Delta V_t| \leq 0.7$ volt throughout the test cycle.

In previous work at Texas Instruments, standard stress test conditions have been ambient temperatures of 175°C and 300°C with an oxide field strength of 1 x 10^6 volt/cm. It is thus of interest to learn whether the relatively poorer stability performance of this group of devices compared with previous results was due to the

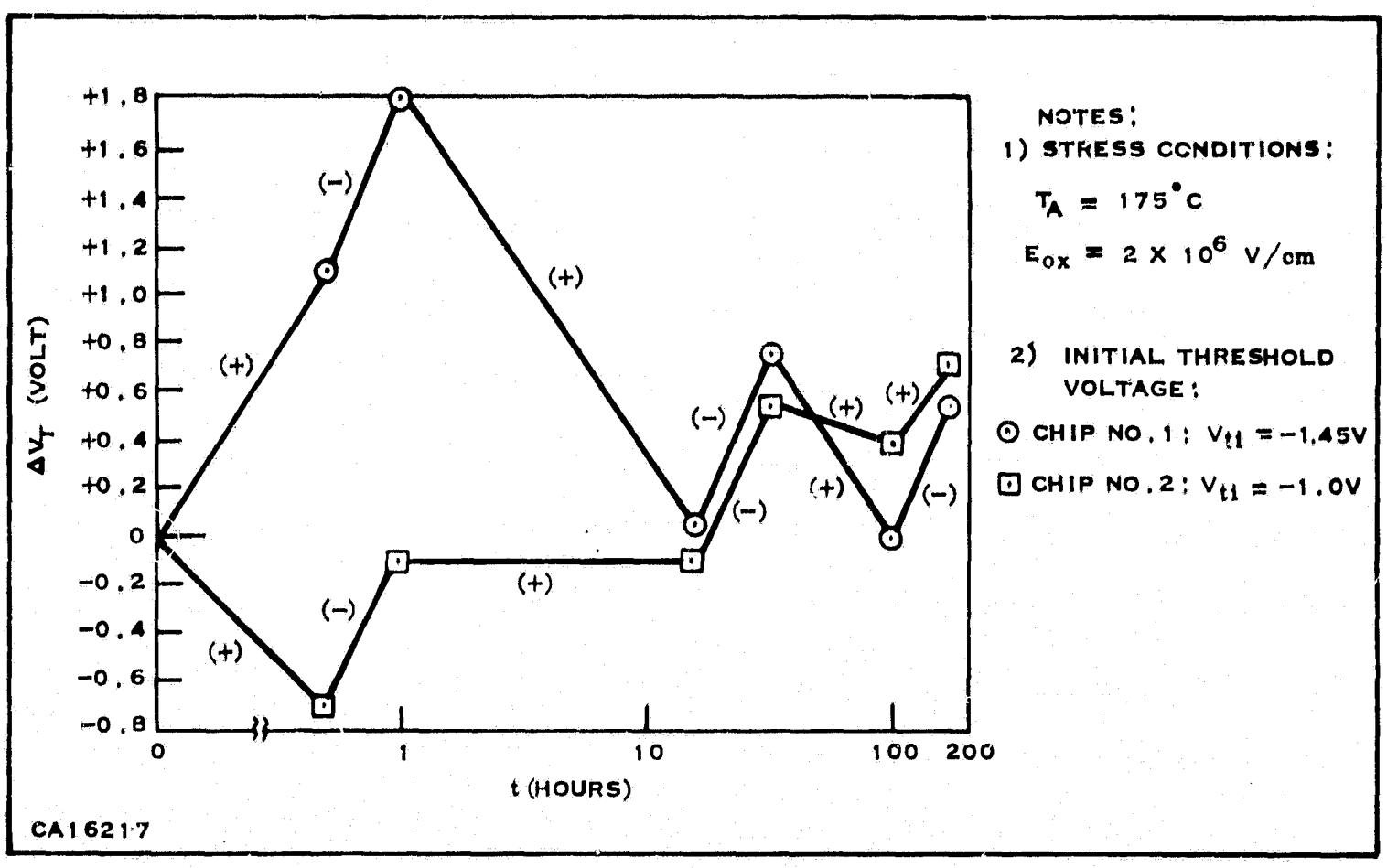


Figure 13. NASA Circuit Transistor Threshold Voltage Stability, Test Cycle No. 2

higher electric field stress in the above described tests or to lower device quality in this run. Two further tests were performed to elucidate this point. In the first, devices from this group were stressed with T_A = 175°C and E_{ox} = 1 x 10^6 volt/cm. In a series of three checkpoints including both gate bias polarities during a 17 hour test, a maximum ΔV_t of 0.7 volt was observed. This is the same level of instability observed on the higher field stress test described above. Second, devices were stressed at 300°C with a field of 2 x 10^6 volt/cm in the oxide. With 7 checkpoints in an alternating polarity test covering 4 hours and 10 minutes, a maximum ΔV_t of 0.9 volts was observed before the device open circuited due to purple plague formation. It is thus concluded that under these highly accelerated stress conditions, the level of instability displayed is not a strong function of either temperature or gate insulator field strength and that hence the stability level of devices from this group are inferior to those of other runs. However, the level of instability observed, $\Delta V_t \sim 0.7$ volt, is quite comparable to that exhibited by group NITP-15, made by a less well-refined technology. This performance was considered quite good at the time.

The material group processed immediately following the run from which circuits were supplied had a very low yield of good devices. Microscopic examination

revealed a high density of pinholes, probably caused by use of a faulty photoresist mask. A very small number of devices were available for testing, however, The results of a 300°C, $E_{ox} = \pm 1 \times 10^6$ volt/cm, 3 hour stress test are shown in Figure 14. The maximum ΔV_t observed is less than 0.15 volt. Unfortunately, no good circuits were found in the material, because of the pinhole problem. The result of this stress test tends to affirm that there is no basic instability problem with the thin insulator technology employed. Similar stability results have been obtained when this technology has been applied to other MIS integrated circuits fabricated within Texas Instruments. The process control problems typical of a laboratory procedure remain to be solved.

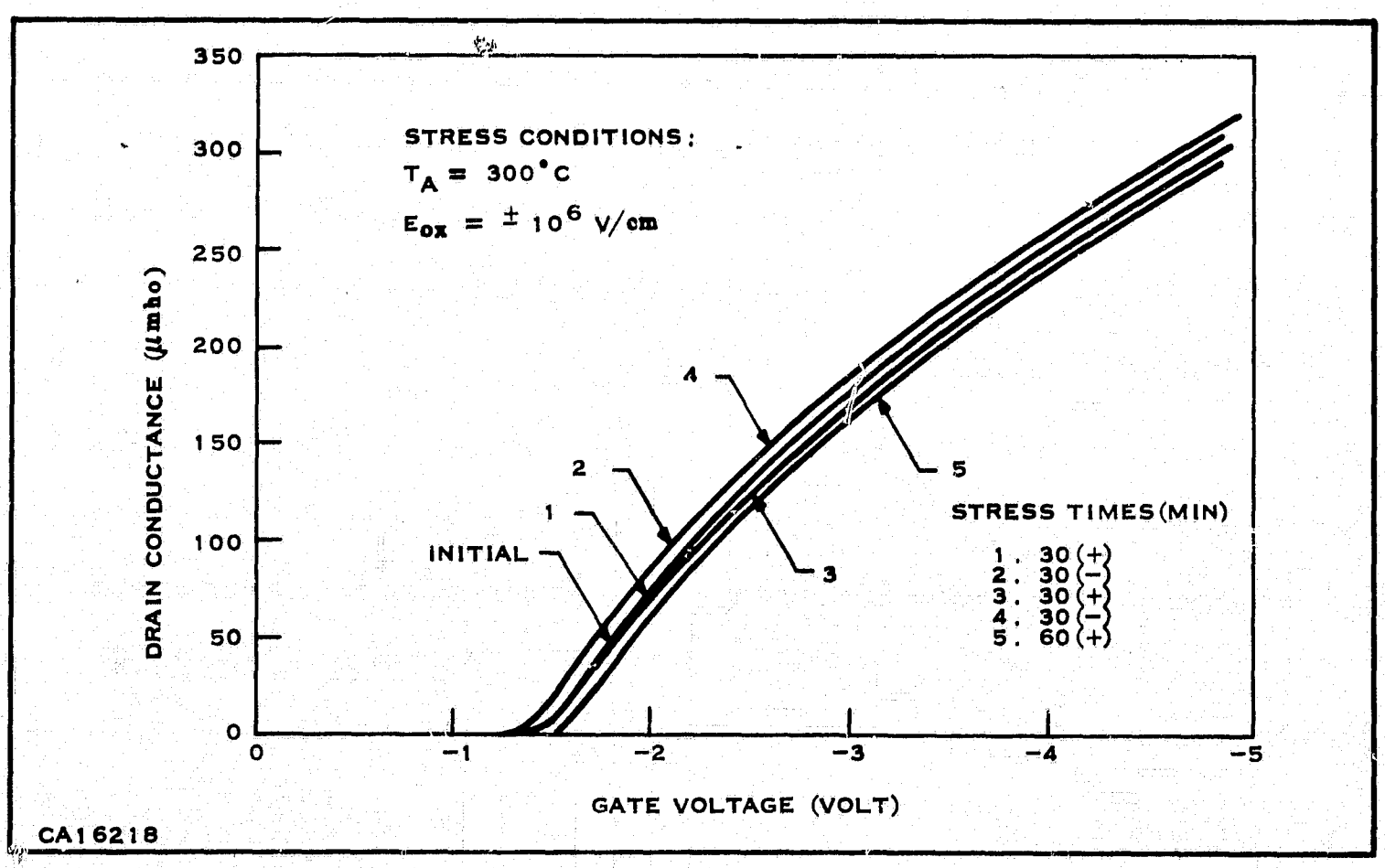


Figure 14. Metal—Nitride—Oxide—Silicon Field Effect Transistor Drain Conductance versus Gate Voltage

SECTION III

FORMATION AND PROPERTIES OF THIN FILM Cr-SiO RESISTORS

The order followed in this section of the report is first an introductory section on the material properties and methods of formation of resistors compatible with silicon device technology. This is followed by a survey of the current literature to form the basis of a comparison with the method used under this contract to form a Cr-SiO evaporated thick film resistors. Finally a brief summary is made of the results under this contract, and suggestions are made for areas in which further investigation is needed.

A. LITERATURE REVIEW

1. Survey of Resistor Types

Much of the material in this section has been obtained from the excellent survey on resistors for Integrated Circuits by the Research Triangle Institute.

In the area of functional electronic block technology, the resistors in the circuit must pass the restriction of compatibility of the two technologies. Two general categories that successfully satisfied this are silicon and thin film resistors.

We shall consider first the general category of silicon resistors of which there are many types that may be used in various integrated circuit technologies.

a. Bulk Resistors

In some respects this is the simplest resistor form available requiring only the application of two contacts to a single-crystalline bar of silicon. The range of useful resistor values obtainable is somewhat limited, particularly those with a low temperature coefficient of resistance, TCR. The nature of silicon is such that TCR increases rapidly with resistivity, limiting low TCR values to highly doped material. A further restriction is the need for electrical isolation. In all, this type of resistor represents an obsolete technology not meriting further consideration.

b. Diffused Resistors

The diffused resistor is probably the most commonly used form of resistor in current use in integrated circuit technology. It is a thin layer resistor and

is formed by diffusing a junction into bulk silicon and making ohmic contact at two points in the layer. In NPN transistor technology, boron doped resistors are commonly formed during the base diffusion step. The junction formed by the diffusant also provides d.c. isolation between the resistor and the substrate, but requires voltage of appropriate value and polarity to be maintained under reverse bias. The primary advantage of this type of resistor over the bulk type is that the thickness $t = x_j$ can be readily fabricated one to two orders of magnitude less than that of the bulk type, hence low values of resistivity, with more favorable TCR, can be used to attain reasonable values of sheet resistance. The other dimensions, length and width, can be controlled by accurate photolithographic processes.

c. Epitaxial Resistors

This form of resistor is not presently in general use. Its fabrication is more complex than that of diffused resistors, and it tends to have a higher value of TCR. The reason for this is that for a particular value of resistivity, the diffused variety is more compensated, and exhibits carrier ionization from the compensated levels at lower temperatures than would occur for band to band excitation in the uncompensated epitaxial material. This increase in carrier concentration counteracts the increase in resistance due to lattice scattering, resulting in a lower TCR than in the epitaxial material.

d. Vapor Deposited Silicon Resistor

This resistor is formed by the same process as the epitaxial resistor except that the deposition is made onto thermal SiO_2, generally in a polycrystalline form. Photolithographic techniques may be used to define the geometry. Resistance vs. temperature behavior is seen to resemble that of bulk polycrystalline silicon. Also, increased doping displays lower TCR. In general, the large density of grain boundaries of the vapor deposited polycrystalline silicon resistor results in lower values of the TCR than for similarly doped epitaxial layers. Values of TCR as low as 150 ppm/°C over the temperature range -50°C to 150°C have been observed on polycrystalline layers, whereas single crystal layers are generally ~ 220 ppm/°C. (17)

e. Series or Parallel Combination

In this approach, resistive elements possessing TCR of opposite sign are arranged either in parallel or series to reduce the combined TCR.

f. MOS Resistor

This is a method of achieving a voltage variable resistor of high value. Its primary advantages are small size and perfect compatibility with MOS integrated circuit fabrication techniques.

g. Other Systems

Table (1) summarizes the properties of the above mentioned resistor technologies as well as other systems such as the Impurity Compensated Resistor (gold doped) and Reverse Biased p-n Junction.

h. Thick Film Resistors

Thick film resistors are capable of fabrication up to very high values of sheet resistance, 300,000 ohms/square. The constituent material of thick film resistors is a cermet mixture of particles of metal and dielectric. Thick films are of often deposited by a silk screening technique or spraying, and require firing at temperature of about 800°C. This alone can render the technique incompatible with many integrated circuit processes, in addition to which there is the general restriction of geometrical definition to line widths 5 mils or larger. Attempts to overcome this by using high resistivity mixtures tends to result in large TCR. Contacts by thin metal films to thick cement films also are a source of problems.

i. Thin Film Resistors

(1) Factors Affecting Resistivity

Although the diffused resistor is the form most commonly used in present-day integrated circuit technology, the thin film approach is rapidly gaining in recognition. With successful solution of its complex fabrication problems, the natural advantages of this technique will undoubtedly prevail. Some of these advantages:

Capability of fabrication over a greater range of values.

Increased precision.

Lower TCR.

Reduced Parasitics.

Current research in thin film technology is primarily concerning itself with (1) the development of desirable electrical characteristics and (2) adequate control of fabrication processes to achieve these characteristics consistently. Probably the most important characteristics are film resistivity and TCR. Other important properties that are usually under consideration are for example, stability of electrical characteristics under electrical, thermal and environmental stress (this would include

Table 1. Types and Properties of Silicon Resistors [16]

Type	Max. Reasonable ρ_s (ohms/□)	Typical Tolerances (%)	Min. TCR (ppm/°C)	Advantages	Disadvantages
Bulk	10^4	±30%	High ($>10^3$)	1) Easy to build 2) Certain interconnections internally made	1) Very high TCR 2) Poor tolerance 3) Additional isolation often required
Diffused	10^3	±10%	200	1) Good dimensional control 2) Flexible size and shape 3) Junction isolation possible by operating voltages	1) Dependent on large area p-n junction for isolation 2) Capacitance of isolating junction added to circuit
Epitaxial	2×10^3	±15%	200	1) Nearly homogeneous impurity distribution	1, 2) Same as for diffused layer 3) Geometry must be defined by additional diffusion 4) Limited to the impurity concentrations obtainable by vapor deposition
Vapor Deposited Layer	–	–	100–150	1) DC isolation is independent of operating voltage and polarity 2) Less capacitive coupling than junction isolated resistors	1) Adherence and uniformity poorer than epitaxial layer 2) Capacitance of MOS structure added to circuit 3, 4) Same as for epitaxial layer
Series or Parallel Combination	–	–	–	1) Reduces TCR	1) Analysis is difficult 2) Reproducibility poor
Compensated Impurity Resistor	High ($>10^4$)	–	Low (<300)	1) High sheet resistivity with low TCR	1) Fabrication technology is not presently available

Table 1. Types and Properties of Silicon Resistors (Continued) [16]

Type	Max. Reasonable ρ_s (ohms/□)	Typical Tolerances (%)	Min. TCR (ppm/°C)	Advantages	Disadvantages
Reverse Biased Junction	10^3 to 10^{10} Ω Resistance	–	High (?)	1) High values of resistance 2) Small area	1) Control is not yet demonstrated 2) TCR may be high without some form of temperature compensation 3) DC and ac resistances may be quite different
Channel Resistance of FET	10^8 Ω Resistance	–	High	1, Same as reverse biased 2) junction 3) Well established technology	1) Restricted operating ranges 2, Same as reverse biased 3) junction

overload tolerance), compatibility with technology of the host circuit, ease of accurate fabrication and definition.

Some of the important factors that contribute significantly to the resistivity of a thin film are discussed below.

(a) Composition

The contents of this report will show that this is probably the most significant factor affecting film resistivity frequently manifesting itself in problems associated with lack of its control. The effects of impurity and environmental (ambient) contamination also fall under this category. Accurate compositional analysis is usually difficult, frequently incomplete and therefore often of little value. For example, oxygen content can be a most potent constituent, yet be virtually undetectable.

(b) Film Thickness

Three distinct regions of resistivity dependence upon film thickness have been observed [18]. The first region is that in which the resistivity is that of the bulk material. The film thickness of this region must be greater than 1000Å. For films in the second region, with thickness in the hundreds of angstroms range, the resistivity increases over the bulk resistivity and the TCR approaches zero. The third region, corresponding to the thinnest films (less than several tens of angstroms), is characterized by a very high resistivity and a negative TCR. The following equation is generally used to describe the resistivity of a thin film as a function of the bulk resistivity:

$$\rho_f = \rho\,(1 + A/t)\ ,$$

where ρ and ρ_f are the resistivities of the bulk and the thin film material, respectively; t is the film thickness; and A is a constant which is a function of the mean free path of the electrons. The value of A is usually determined experimentally for a particular film.

(c) Thermal History

The effect of heating upon the resistivity of a thin film is often quite pronounced and somewhat unpredictable. Mechanisms responsible for these changes are thought to be annealing, agglomeration and corrosion [19]. The annealing action removes vacancies, dislocations, and occluded gas pockets from the film, changing the resistivity.

Agglomeration, which describes the gathering into small islands that certain films have been observed to undergo with heating, greatly increases the film resistance. This redistribution of material occurs for films only several hundred angstroms thick at temperatures slightly above the recrystallization temperature of the metal of the film. Most metals oxidize before agglomeration occurs. Three notable exceptions are gold which agglomerates at about 450°C, platinum which agglomerates at about 600°C and silver which agglomerates at about 300°C.

The effect of corrosion is also to increase the film resistance since the chemical reaction usually form a metallic oxide or other salt. At 600°C corrosion deteriorates all films except platinum and gold. A layer of silicon monoxide or other overcoating can afford some protection against corrosion.

Table 2 lists the resistivity and TCR of various metal films.

A more recently observed phenomenon (20) accounting for complex annealing phenomena in cermet resistors is thought to be equilibrium formation of compounds from the deposited constituents stimulated by the annealing process.

(d) Deposition Method

Even with perfect compositional control, the actual deposition method can have a profound effect on film resistivity. Consider the differences between cermet films deposited by flash evaporation as compared to coevaporation. In the former, intense high temperature and chemical reaction between the constituents can occur, whereas in the case of coevaporation, the constituents are deposited separately onto a relatively cold substrate with minimal chemical reaction. Chemical interactions as well as the effects of diffusion can be vastly different.

The degree of dispersion of the constituents, assuming some agglomeration or crystallization occurs, can have a profound effect on resistivity. If the dielectric has a characteristically high atomic mobility, the metal species will agglomerate into large islands, widely spaced, resulting in an insulator. SiO and SiO_2 have the property of restricting this phenomena, which is one reason they are so frequently mentioned in the cermet literature. A considerable amount of earlier thin film work was concerned with the properties of metal films, some of which are characterized in Table 2. One of the characteristics of a metal film is the relatively low value of sheet resistivity attainable. Only by making the films extremely thin

Table 2. Resistivity and TCR of Various Metal Films* [19]

Metal	ρ_f (before annealing)	ρ_f (after annealing at 600°C)	TCR	Bulk TCR (0–100°C)	Ratio of Film TCR to Bulk TCR
Au	22.2	4.95	2800	3400	0.82
Pt	8.7	15.65	2500	3900	0.64
Ir	12.8	42.5	1800	4000	0.45
Rh	17.3	15.8	2000	4600	0.43
Pd	20.3	20.8	2300	3700	0.62
Ni	28.5	41.0	5000	6400	0.78
Cr	172.5	62.0	600	–	–
Ti	67.1	59.9	700	5400	0.13
Zr	134.0	–	<100	4400	0.02
Mo	99.5	49.0	200	3300	0.06
Ta	768.0	–	<100	3100	0.03
W	4390.0	422.5	<100	4800	0.02
Al	0.41	0.36	2800	4300	0.65

*Units are: ρ_f ohm-cm
TCR ppm/°C.

(less than 100Å) does the sheet resistivity rise to high values (greater than 1000 ohms/square). The added control problems in doing so lead to poor reproducibility and unsatisfactory performance. Generally, the maximum practical limit of sheet resistivity is set in the vicinity of 200—600 ohms/square.

(2) Evaporated Nichrome Resistors

Nichrome has been frequently used to form resistors in integrated circuits (21-26). It is frequently used in radiation hardened circuits. Deposition is usually either by tungsten heater or E-gun. The films are defined by masking during deposition or later by photolithography. Film thickness, substrate temperature, and aging are important parameters as shown in Figures 15 and 16. The relatively advanced state-of-the-art for building resistors from nichrome film makes this technique attractive. For other reported values of evaporated and sputtered Ni-Cr resistors, see Figure 17 which shows data for sputtered and evaporated Ni-Cr from the AGED symposium on passive film components. It should be noted that the data for sputtered nichrome strongly suggests continuous metallurgical morphology, as there is no apparent change in TCR with decreasing thickness.

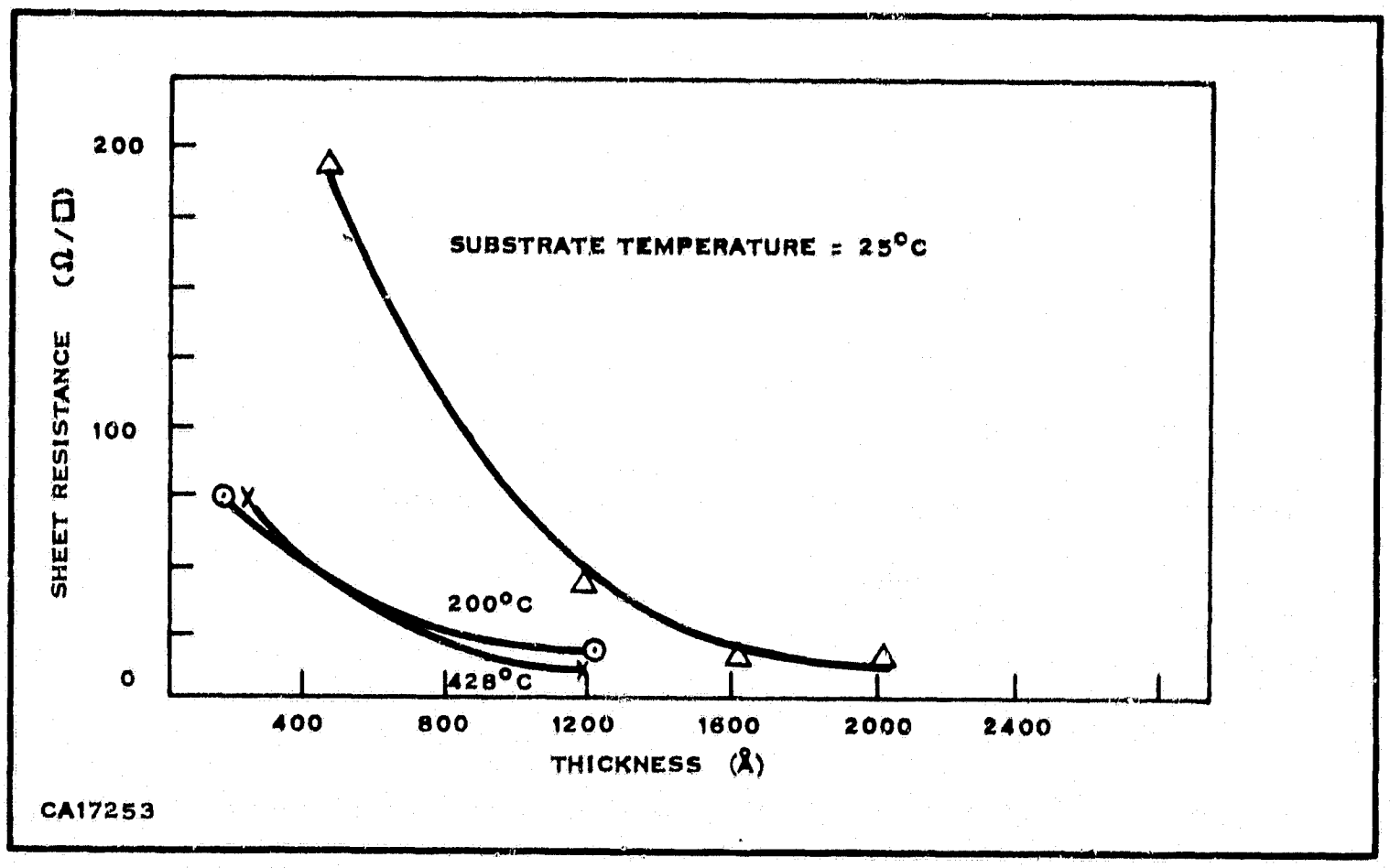


Figure 15. The Dependence of the Sheet Resistance of Nichrome Resistors Upon Thickness and Substrate Temperature [22]

(3) Tantalum Resistors

The data shown in Table 2 shows tantalum to have a reasonably high sheet resistivity and low TCR. Sputtering is the preferred deposition method because of its refractory nature. The oxidation of tantalum produces protective oxide with a concomitant resistivity increase. Stabilization is adequate at a temperature in excess of the operational value. Resistance versus time and temperature curves have been developed and can be used to controllably trim to spec. Resistors aged at 250°C in air have been shown to change their value by only 1% after operation at 150°C for 2000 hours.

(4) Other Systems

Other systems that have been studied but whose use in microcircuit technology is questionable are (1) electroless nickel, where the primary advantage would appear to be the freedom from dependence on expensive vacuum processing, and (2) tin oxide, where the main disadvantage appears to be the necessity for a 1000°C–1200°C processing step.

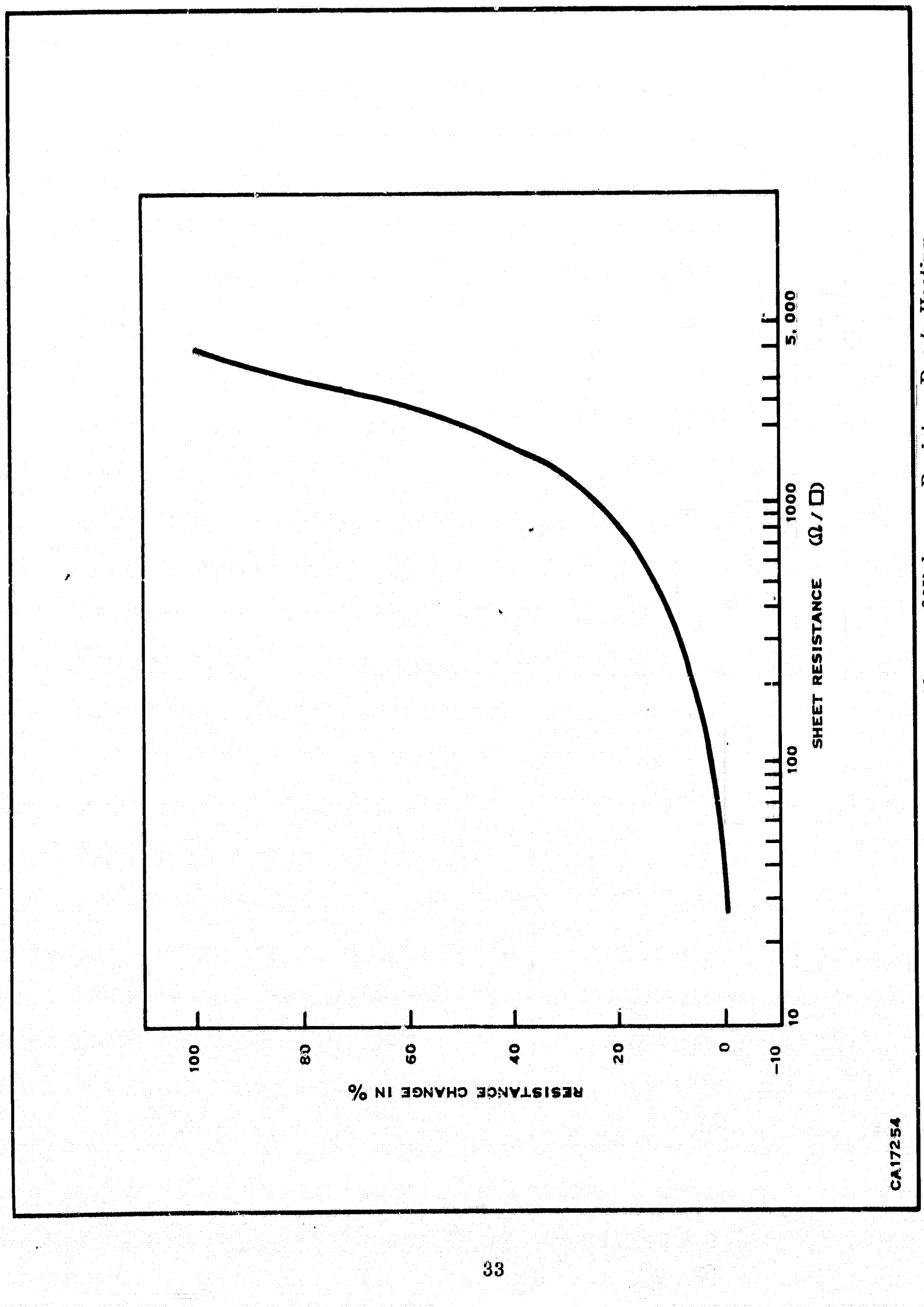


Figure 16. The Resistance Change of Nichrome Resistors Due to Heating in Air at 250°C for 10 Minutes Versus Sheet Resistance [18]

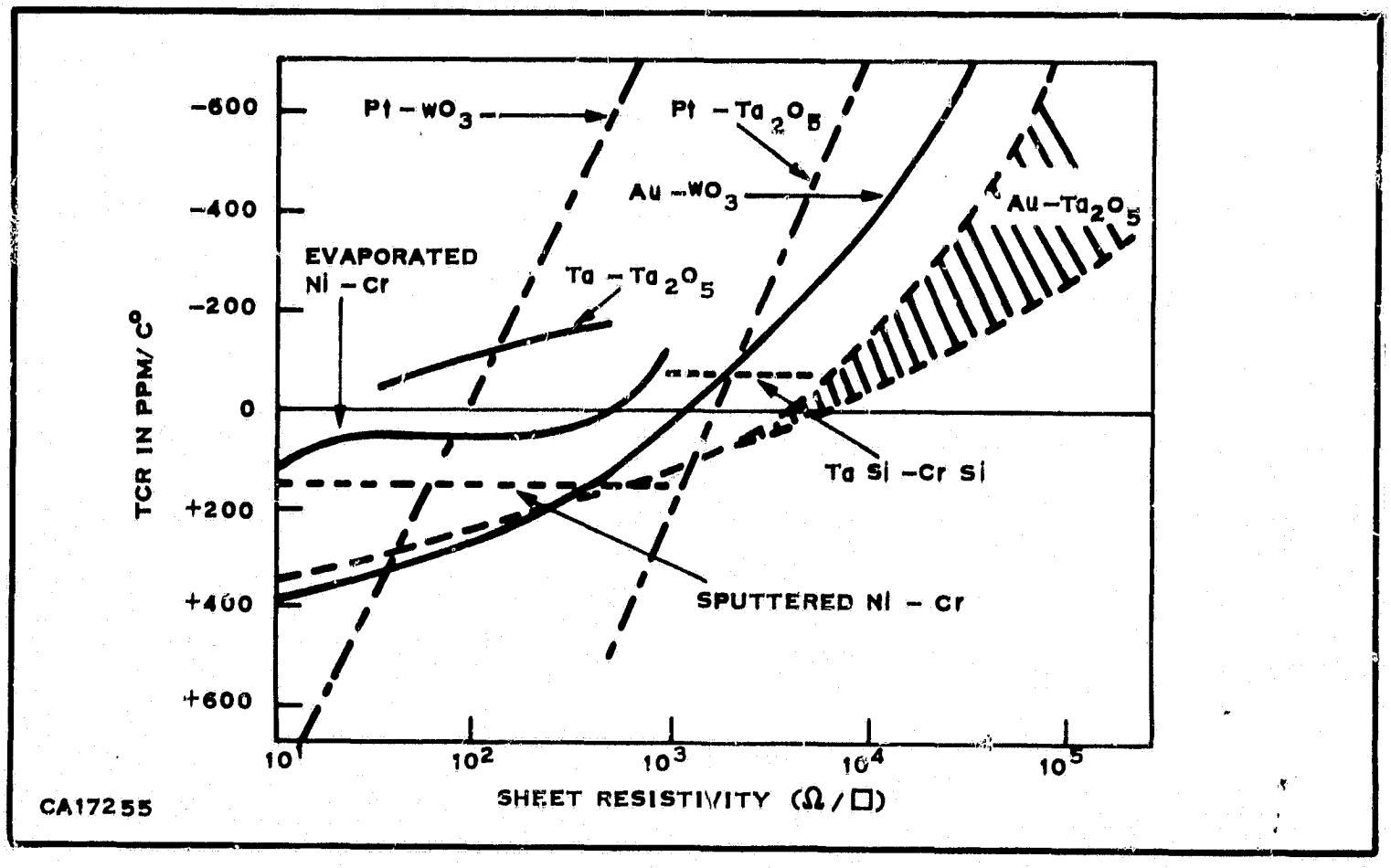


Figure 17. Comparison of Cermets Produced by Reactive Sputtering to Other Film Resistors [39]

(5) Cermets

Early work on cermets (27) reported in 1959, was not too encouraging. Cr-SiO_2 resistors were deposited on glass substrates by simultaneous evaporation of chromium and SiO_2. The resulting resistors exhibited considerable instabilities at 25°C, Table 3. Although a perusal of the literature will show wide variance in data, considerable improvement has been achieved lately, in terms of stability, control and understanding. The potential metal-dielectric cermet combinations is large indeed, and many systems have already been studied by a variety of deposition methods. Figure 17 compares the sheet resistivity dependence of TCR for a variety of different film resistor materials, Ni-Cr, Ta-Ta_2O_5, TaSi-CrSi, Pt-WO_3, Pt-Ta_2O_5, Au-WO_3 and Au-Ta_2O_5. Recently, exotic mixtures such as Ta, Si, Cr, Al_2O_3 (28) have been under investigation.

Cr-SiO cermets have been shown to have excellent stability characteristics both under thermal stress and storage, as well as humidity. There is evidence in the literature that zero TCR can be controllably achieved in a limited though useful range of bulk resistivity, which is considerably higher than generally

Table 3. Resistance Change of Chromium-Silicon Dioxide Cermet Materials While Aging at 25°C [27]

Resistor No.	Initial Sheet Resistance (ohms/□)	Total Increase After 8 Days (%)	Total Increase After 28 Days (%)	Approx. Film Thickness (Å)	Avg Temp Coef of Resistivity (ppm/°C)	Approx. Stability of Nichrome Resistors of About the Same Sheet Resistivity
R_2	230	- 2	+ 5	1625	-320	
R_3	200	- 2.5	± 0	1520	0	+10% after 7 days
R_4	540	+ 2.0	+ 3.0	168	-280	
R_5	1780	+ 4.0	+ 5.2	113	-250	+25% after 2 days
R_6	2950	+10.0	+11.5	100	0	+50% after 7 days

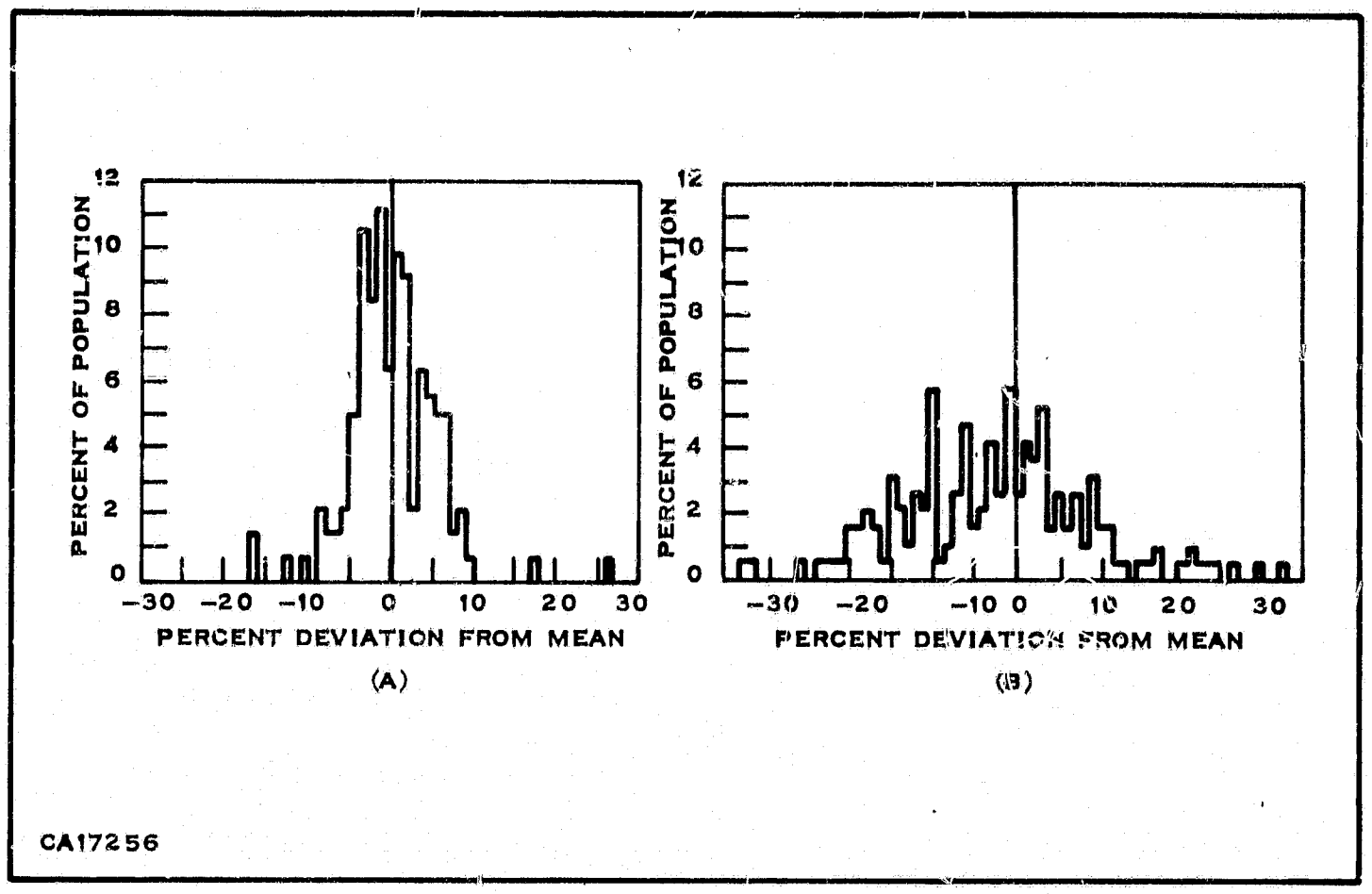


Figure 18. (a) Distribution of 1-Mil Wide Cermet Resistors
(b) Distribution of 1-Mil Wide Diffused Silicon Resistors [29]

obtainable from metal and alloy films. The ensuing higher sheet resistance values attainable in practice afford considerable reduction in area requirements of the resistor portion of an integrated circuit.

The recent improvements in control apparently result in increased precision and reproducibility in fabricated resistor values. For example, Braun and Lood (29) show the superior precision obtainable with 1-mil wide cermet as compared with diffused silicon results. See Figure 18.

It appears that the present state-of-the-art in thin film Cr-SiO cermet resistor technology is at the threshold of a final maturing phase. Other cermet systems are under intensive study but at present should be categorized in the research stage.

2. Methods of Deposition of Cermet Thin Film Resistors

There are various ways in which thin film cermets may be deposited:

Simple boat evaporation of the constituents

Simultaneous coevaporation of the constituents from separate sources

Powder flash evaporation

Pellet flash evaporation

DC and rf sputtering metal and dielectric.

These various methods will be discussed in the following sections.

a. Simple Boat Evaporation

Early work on Cr-SiO_2 cermets (27) is summarized in Table 3. The resistors were fabricated on glass microscope slides by simultaneous evaporation of chromium and silicon dioxide in an approximate ratio 80:20. Substrate temperature was 450°C, and bell jar pressure 2×10^{-4} torr. of oxygen. Following deposition, the resistors were annealed at 450°C for one hour in an atmosphere of 2×10^{-4} torr. oxygen. The table shows that the resulting resistors were very unstable, even at room temperature. Improvements were later obtained by flash evaporating 70 at % Cr, 30 at % SiO, 0.5 % by wt, colloidal SiO_2 with the substrate held at 220°C, p = $5-10 \times 10^{-5}$ torr. The resulting stability was a considerable improvement, and the sheet resistance was 250 ohms/square. Attempts to achieve higher sheet resistance values encountered control problems.

Pitt (30) describes properties of cermet resistors produced by evaporation of Cr and SiO from tantalum boats in the composition range 40%–60% Cr. Deposition was at $2-3 \times 10^{-5}$ torr. with glass substrates maintained at 380° C. Resistors were defined by metal shadow masks. Contacts were nichrome-gold. Resistance ranges investigated were 200–2200 ohms/square. Post-deposition resistance changes were observed which include the effects of air age as shown in Figure 19. They range from less than 10% at low sheet resistance to approximately 70% at 2200 ohms/square. Films obtained ranged from 300 ohms/square, 400Å thick to 2500 ohms/square, 1000Å thick films with corresponding volume resistivity in the range 10^{-3} to 2.5×10^{-2} ohm-cm. No direct measurement of SiO content in the films was made, but it is less than that of the starting material. An increase in the scatter of resistance, TCR and noise values was noted for increasing sheet resistance. However, TCR was generally in the range $\pm$125 ppm/°C, and noise was low. In cases of low aspect ratio geometries, contacts were found to contribute negative TCR. Stability under thermal and humidity stress was good. Resistance control appears to be the primary problem in this investigation, primarily due to resistance increase in air. In the higher resistivity ranges, fabricated resistor values range +60 to −20% from target value.

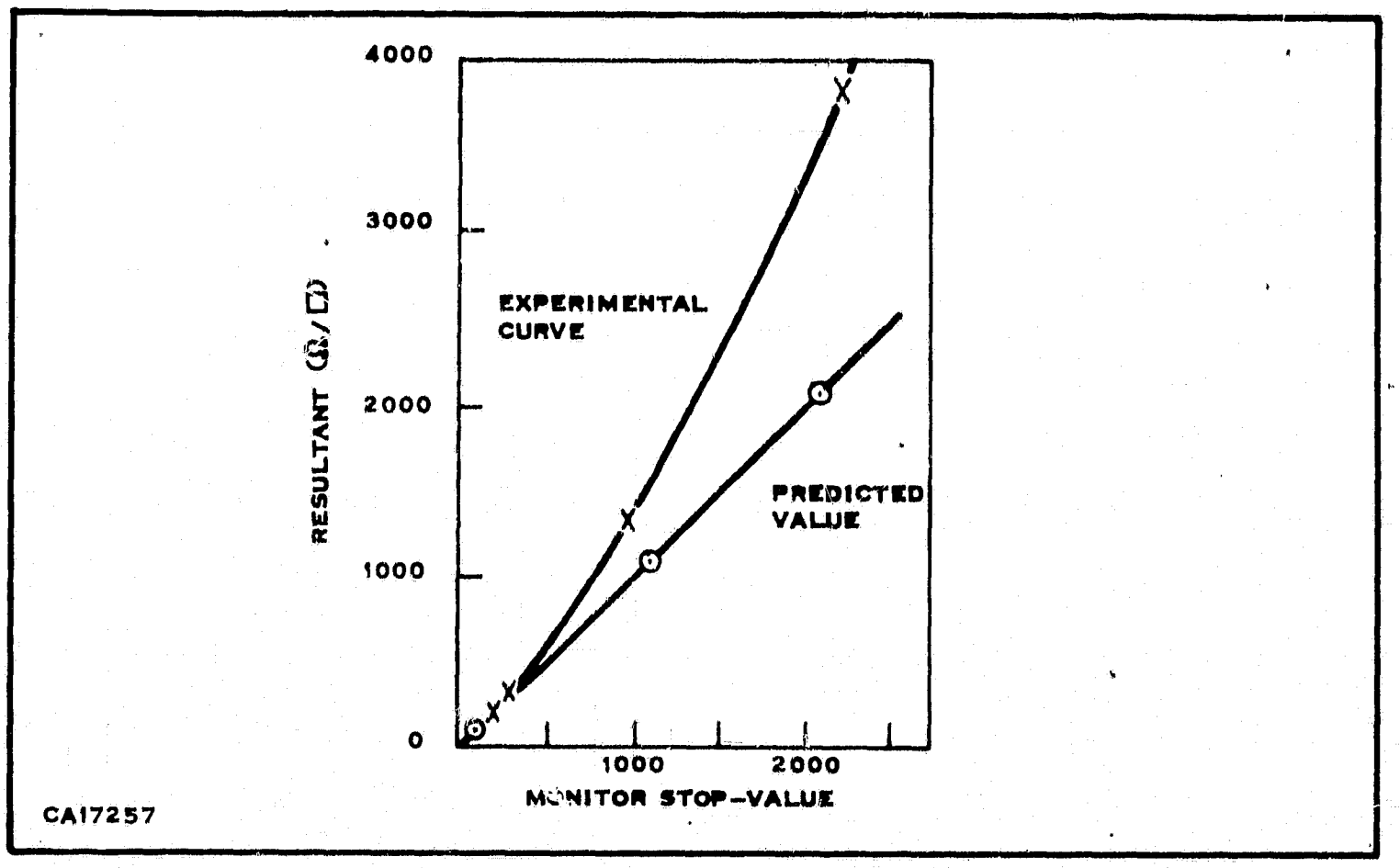


Figure 19. The Relationship Between Initial Monitor Values and Final Resistivity [30]

b. Coevaporation from Separate Sources

Cermet films may be deposited by simultaneous coevaporation of the constituents from two separately controlled sources. The primary advantage of this method is (1) the basic freedom to vary the compositional ratios of the constituents, and (2) permitting deposition without solid phase reaction of the components. This latter may or may not be desirable. A disadvantage is the complexity of the control problem.

Simultaneous coevaporation of the constituents has been studied by Beckerman and Thun (31) and by Ostrander and Lewis (32). Beckerman and Thun utilized two independently heated sources (resistance heated, RF heated and E-gun) each controlled through feedback loops by ion gauge rate monitors. Compositional control of $\pm$1–2% is claimed by this method. Four metal-dielectric systems were studied. Au-MgF_2, Au-SiO, Cr-MgF_2, Cr-SiO in the following atomic % concentration ranges for the metal species: Au-MgF_2 = 60–90%, Au-SiO = 40–90%, Cr-MgF_2 = 65–98%, Cr-SiO = 45–90%. Au-MgF_2 and Au-SiO suggested that SiO was a superior dielectric to MgF_2 for cermet applications due to its apparently lower atomic mobility which inhibits migration and ensuing agglomeration of the metallic species. This maintains bridging between smaller islands resulting in more uniform dependence of resistivity upon metal-dielectric ratio. Cr-SiO deposited at 320°C also showed better stability than the MgF_2 combinations.

Ostrander and Lewis (32) used a coevaporation technique to study the effects of compositional variation on electrical properties. The chromium was used in the form of a coated strip, resistance heated to 1500° C. The SiO powder was evaporated from a tantalum heated diffusion cell, also resistance heated, to 1100° C. Compositional variation and control was achieved by spacing the two sources 25 cm apart and placing the substrates at different locations in a plane 25 cm away from the location plane of the source. The positional dependence of deposit thickness arises from the cosine dependence of vapor flux distribution. Through the correct choice of source size, temperature and layout, a volumetric compositional variation of 20%–80% was theoretically possible with thickness varying by 10%. The pure deposits were also monitored by separately shadowing one of the flux components during deposition to the exclusion of the other. This served to estimate the deposited volume fractions. The resistivity dependence on composition is shown in Figure 20 together with data representative of other techniques to be discussed below. It will be noted that the two methods, although basically the same, yielded very different results. The coevaporation of Cr and SiO was used by Lood (33) to study electrical properties of cermets containing 0%–42% SiO by weight. All samples were deposited to a thickness of 300Å at a substrate temperature of 200° C. Annealing is not discussed. Contacts were evaporated gold. Lood confined the study to the interpretation of the behavior of SiO in relatively small amounts (<10%) in Cr and its effect on the two band structure, resistivity and TCR of Cr.

c. Powder Flash Evaporation

Apparently a more desirable evaporation technique is that of powder flash evaporation, where a powdered mix is fed through a hopper mechanism onto a very hot filament, rapidly subliming the material, thus maintaining compositional integrity. This technology is reviewed by Glang, Holmwood and Maissel (34). They describe the work of Beckerman and Bullard (35), Ault (36), Wagner and Merz (37), and Beam and Takahashi (38). They note that the principal problem observed was the difficulty of controlling the room temperature target value of deposited film resistance, imposing the necessity of individualized post-deposition anneals to trim resistance to desired values. It was found that the primary reason for this was the lack of compositional control of the deposit. Since TCR and annealing behavior were very dependent on composition, and the depositions were usually performed with substrates maintained at 200°–450° C, it is easy to recognize the problem in achieving a desired room temperature value for sheet resistance. Much effort was devoted to the problems in the powder feed mechanism where it was felt compositional variations in the mix

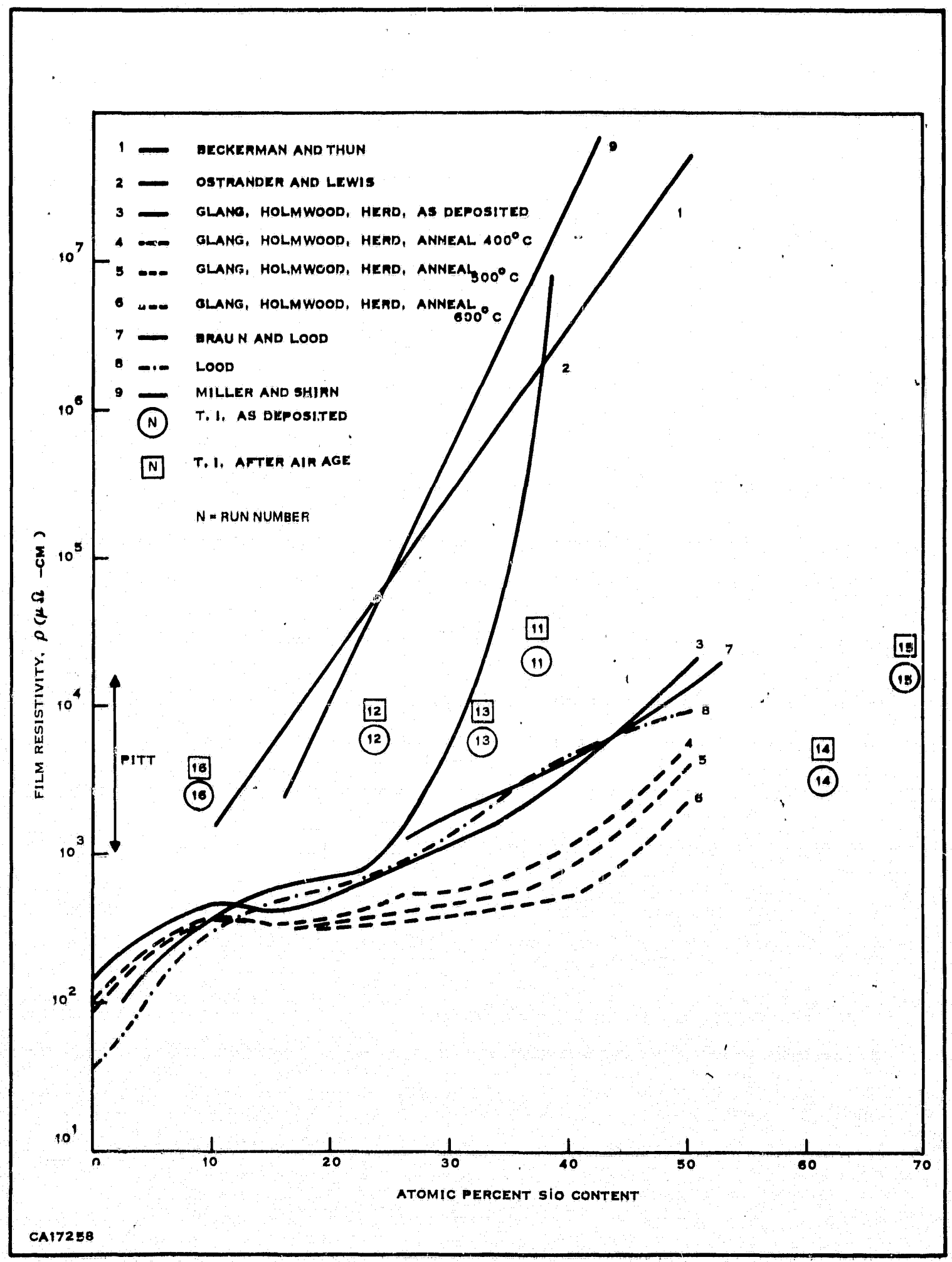


Figure 20. Compositional Dependence of Film Resistivity

occurred, due to a variety of causes such as selective segregation and agglomeration of the powders. The Si-Cr content in these films showed substantial deficiencies in SiO, coupled with poor reproducibility, e.g., SiO content variations from 2 to 22% for a charge mix containing 30% SiO, and from 5 to 35% for 60% SiO source material.

A further mechanism found responsible for these changes was the incipient vaporization of SiO particles in the descending mixture and their deflection before reaching the hot filament surface. This phenomenon arises because of the relatively high vapor pressure of SiO, which is about 1 atmosphere at the 2000° C temperature of the filament. SiO has also been seen to decrepitate upon sudden heating so that a significant fraction of the material is ejected in particulate form after contact with the hot filament. Pitt (30) also describes deflection of the powder feed and its reduction by application of negative bias to the filament.

Braun and Lood (29) used the powder flash evaporation technique to investigate Cr-SiO films in the composition range 53%–77% Cr by weight. The resistivity dependence on composition is shown in Figure 20 compared to other results in the literature. Compositional control was poor due to loss of SiO from the hot filament, as mentioned by Glang, Holmwood and Maissel (34). Desired values of deposited sheet resistance were achieved by post-deposition anneal at the substrate deposition temperature, 400°C. Deposition pressure was $2-3 \times 10^{-6}$ torr. Final film resistivity control was ± 20 percent. Resistors are defined photolithographically, contacts are 600Å titanium followed by 10,000Å–16,000Å aluminum and require sintering at 375°C in an inert atmosphere.

The paper further describes the TCR obtained for two Cr-SiO compositional ratios, see Figure 21, the good precision obtainable from this method and a method for trimming to $\pm 0.1\%$ of desired value by electrically removing series and shunt control resistors. Stability and power dissipation capabilities are also discussed.

Powder flash evaporation of Ta, Si, Cr, Al_2O_3 using an E-gun source was described by Terry (28). During deposition the substrate temperature was 380°–400°C, pressure was $2-4 \times 10^{-5}$ torr. with a deposition time of 165–250 seconds. Air bakes at 450° C resulted in resistance increases of 25%–100% over an aging period of up to 1-1/2 hours. Resistors were deposited intentionally low and air aged to desired values.

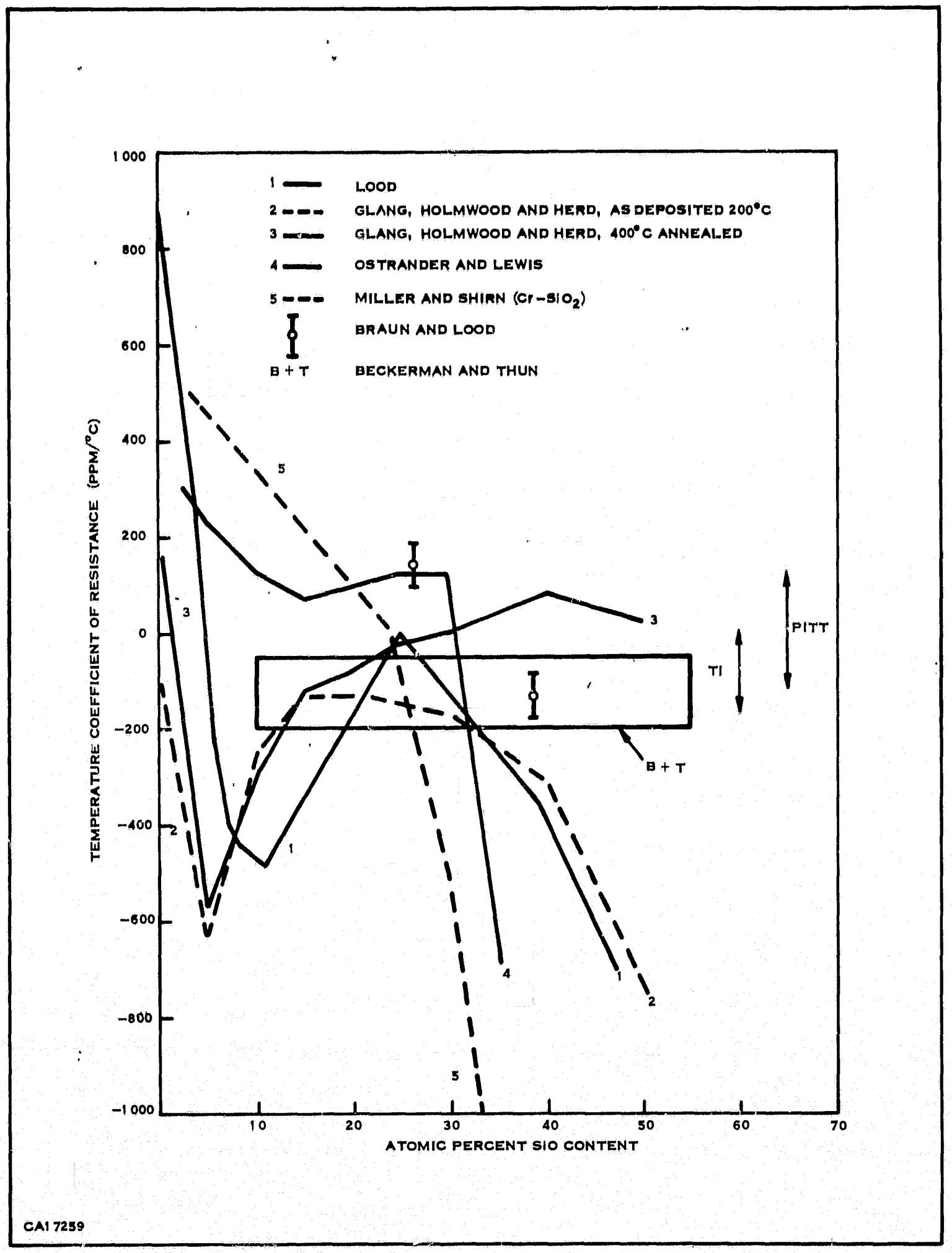


Figure 21. Compositional Dependence of TCR

After thermal trimming distribution of resistor values is about 20% across 1-inch wafer. This was found to be mainly due to geometrical discrepancies experienced in photoresist and etch delineation. A compositional breakdown of the cermet charge was not given.

d. Pellet Flash Evaporation

Glang, Holmwood and Maissel (34) describe a flash evaporation technique which overcomes the above problems by supplying the Cr-SiO in pellet rather than powder form. The pellets were formed by mixing Cr and SiO powders with organic solvents, resin binder and a plasticizer and casting the mixture in the form of thin sheets from which the pellets were cut. The organic materials were then removed by heating in air at 500°C and the pellets hardened by sintering at 1100°C in an evacuated quartz capsule.

During flash evaporation, the pellets were fed at a controllable rate via a hopper mechanism to the hot filament. In this fashion, the compositional control problems mentioned above were essentially solved. Since some fractionation always took place, the pellet feed rate was adjusted so that there were always several particles residing in the hot filament at different stages of vaporization. During evaporation the system pressure was about 5×10^{-7} torr. Substrate temperature was always maintained at 200° C. Film thicknesses of 1000Å generally required evaporation times of 40–50 seconds. Deposition resistance was monitored on circular silicon wafers with four preevaporated peripheral contacts after the method of Van der Pauw. Compositional and resistance control were found to be very satisfactory ≤±2 mol % using this method.

Using this technique, Glang, Holmwood and Herd (20) investigated Cr-SiO films from 0 at % to 50 at % SiO and were able to adequately explain the behavior of structure, resistivity, TCR in terms of composition and thermal history.

e. DC and RF Sputtering of Metal and Dielectric

In some respects the sputtering technique is the most attractive method for the deposition of cermets. Some of the better known advantages are:

Ease of deposition of refractory conductors and insulators
Ease of co-deposition control to form range of mixed deposits
Ability to deposit alloys or mixtures without selective depletion of the source
Ability to create dielectric by reactive sputtering
Avoidance of high temperatures
Good adherence to substrate.

Lane and Farrell (39) used a reactive dc sputtering technique involving a dual cathode and rotating substrate holder to deposit various compositions of $Au-WO_{3-x}$, $Pt-WO_{3-x}$, $Au-Ta_2O_{5-x}$, and $Pt-Ta_2O_{5-x}$ ($0 \leq x \leq 1$). The dielectrics were obtained by making one of the dual cathodes either tungsten or tantalum. Their objective was to obtain a cermet with high resistivity and low TCR. Of the four systems studied $Au-Ta_2O_5$ was the most interesting, with zero TCR occurring at 7000 ohms per square. In Figure 17 TCR dependence on sheet resistivity is plotted for all four systems studied together with other data collected by Lane. The $Ta-Ta_2O_5$ was obtained by sputtering tantalum in an argon-oxygen ambient. High sheet resistivity could not be achieved controllably. The TaSi-CrSi was electron beam evaporated. The $Au-Ta_2O_5$ was the most attractive combination from the point of view of electrical characteristics. Unfortunately, there are indications it suffers from gross instabilities under 100°C storage stress. Further study is nevertheless merited.

Miller and Shirn (40) have recently reported a versatile sputtering technique for depositing cermet films. They rf sputter an insulator while simultaneously dc sputtering a conductor. This co-sputtering method is apparently more versatile than coevaporation (or reactive dc co-sputtering) since a much wider range of insulators can be rf sputtered, and alloys can be dc sputtered with no loss in composition. By various arrangements of targets and substrate positions, films can be deposited either with uniform composition determined by the targets or with a smooth gradation from one target composition to the other. Resistivity uniformity of $\pm 10\%$ is claimed. The electrical properties of these films differ substantially from these obtained in most of the evaporation experiments and will be discussed in the section on electrical properties.

3. The Influence of Composition on Structure, Thermal Behavior and Electrical Properties of Cermet Films

The literature shows considerable variation in properties of the Cr-SiO cermet films studied, where the compositions are supposedly similar. There is mounting evidence that the electrical properties exhibit a strong dependence on Cr-SiO composition and structure, which, in turn, are dependent on deposition methods and post-deposition treatments.

In general, film resistivity tends to increase with SiO content. Annealing reduces the metastable condition of the deposit, inducing internal formation of new compounds, formation of solid solutions, disproportionation reactions and possibly reactions with the external ambient.

Some of these points are discussed comprehensively in a recent publication by Glang, Holmwood and Herd (20). The cermet films they studied were fabricated by the pellet flash evaporation method of Glang, Holmwood and Maissel (34) described earlier. Electron microscope studies revealed α-Cr and Cr_3Si as the principal structures. When deposited on cold substrate the films were seen to be entirely amorphous. Elevating the substrate temperature during deposition resulted in increasing crystallinity of the film. First, the chromium crystallized into the α-Cr form. At 200° C weak Cr_3Si patterns could be seen for certain SiO concentrations. Generally, annealing at 400° C was required to crystallize the silicide.

The presence of Cr_3Si and Cr (Si) in solid solution is attributed to the reaction of Cr and free Si arising from the disproportionation of SiO, with the equilibrium structure being governed by the Cr-Si phase diagram, Figure 22, with SiO_2 as an additional constituent. Not all phases indicated in the phase diagram are seen in electron diffraction scans, due to SiO_2 impeding diffusion of the metal species. Hence, only the major constituent is usually seen in electron diffraction studies, as indicated in Figure 23. The dielectric in the equilibrated cermet is deduced to be SiO_2 (not SiO) from the complete disproportionation of SiO that effectively takes place in the formation of Cr_3Si. This reaction is the more probable occurring with little or no change in free energy, whereas the reduction of SiO_2 by Cr has a large positive free energy.

Glang, et al. (20) sum up as follows: the Cr-SiO films tend to condense with very nearly random disorder but are capable of varying degrees of order if subjected to temperatures which afford limited atomic mobility. Depending on the Si-Cr ratio, small crystalline regions of α-Cr or Cr_3Si may form. However, the crystallization of Cr and Cr_3Si is impeded by the presence of SiO_2. Consequently, atomic motion leads mostly to crystallites smaller than 100Å and to metal nuclei with little or no long range order which are "frozen" in the oxide matrix. They surmise that these films are not homogeneous but consist of small particles of chromium and chromium silicide separated by SiO_2. They assumed complete dissolution and disproportionation reactions and were able to calculate the proportional amounts of constituent phases and their relative contributions to the film volume. The resulting composition diagram is shown in Figure 24 which indicates four concentration regions of possibly different electrical properties: up to 5% SiO, the metallic constituent is α-Cr with or without Si in solid solution. From 10% to 30% SiO varying amounts of Cr (Si) and Cr_3Si form a eutectic. Around 40% SiO the films consist of Cr_3Si and SiO_2 and at 50% there exist two phases, Cr_3Si and Cr_5Si_3 in a matrix of SiO_2.

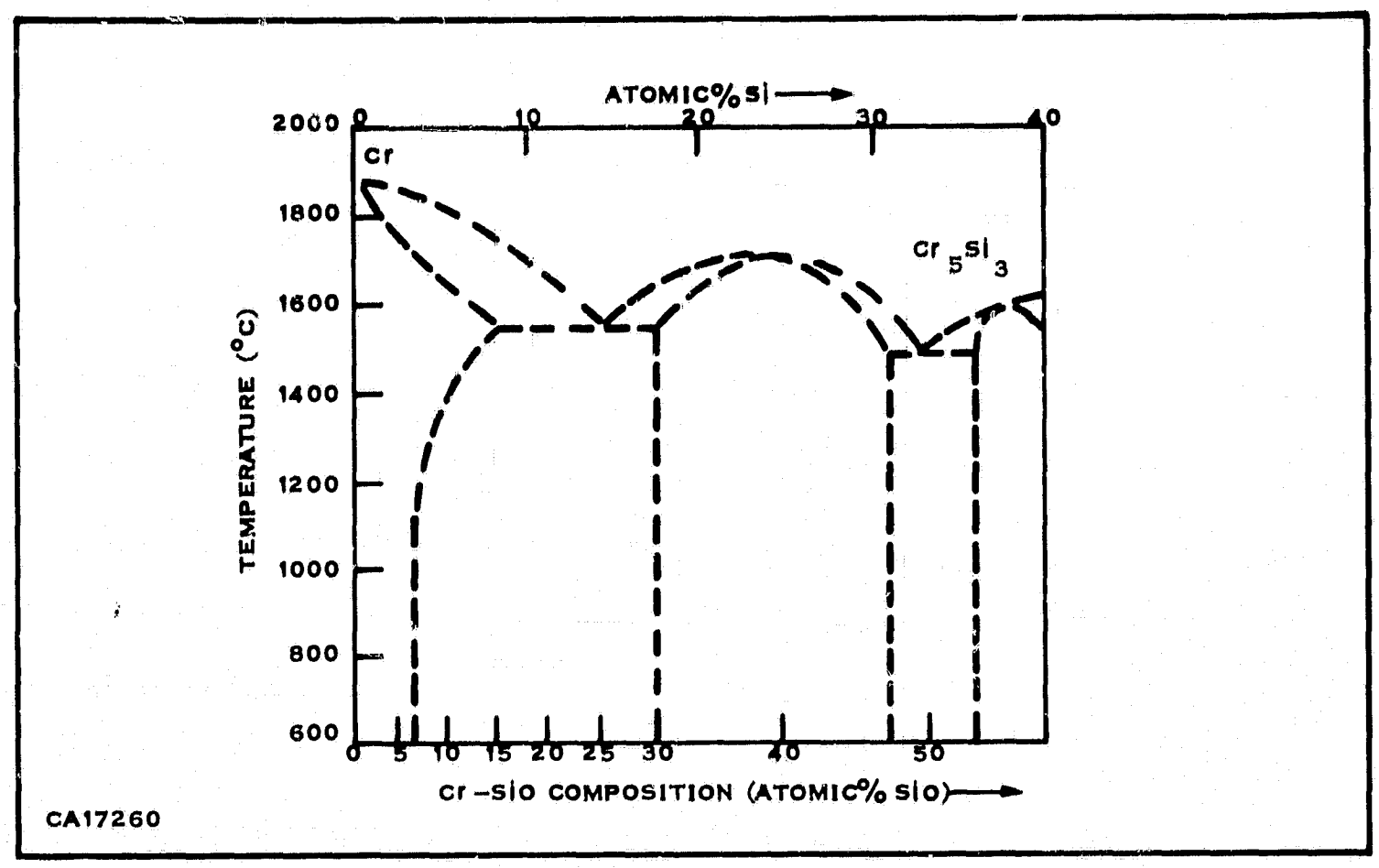


Figure 22. Cr-Si Phase Diagram Indicating Equivalent Cr-SiO Film Compositions [20]

TEMPERATURE OF PREPARATION	CRYSTAL STRUCTURES IN Cr-SiO FILMS (COMPOSITIONS IN ATOMIC % SiO)								
	0	5	10	15	20	25	30	40	50
DEPOSITED AT −196° C	(NOT INVESTIGATED)		NO CRYSTALLINE PHASES						
DEPOSITED AT 25° C	α-Cr								
DEPOSITED AT 200° C									
ANNEALED AT 400° C							Cr_3Si		
ANNEALED AT 600° C									*)
PHASE DIAGRAM (ELLIOTT)	Cr (Si)		Cr (Si) + Cr_3Si					Cr_3Si	*)

$Cr_3Si + Cr_5Si_3$ (C)

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Figure 23. Crystal Structures of Cr-SiO Films of Various Compositions Observed After Different Thermal Treatment. Annealing times: 1 h [20]

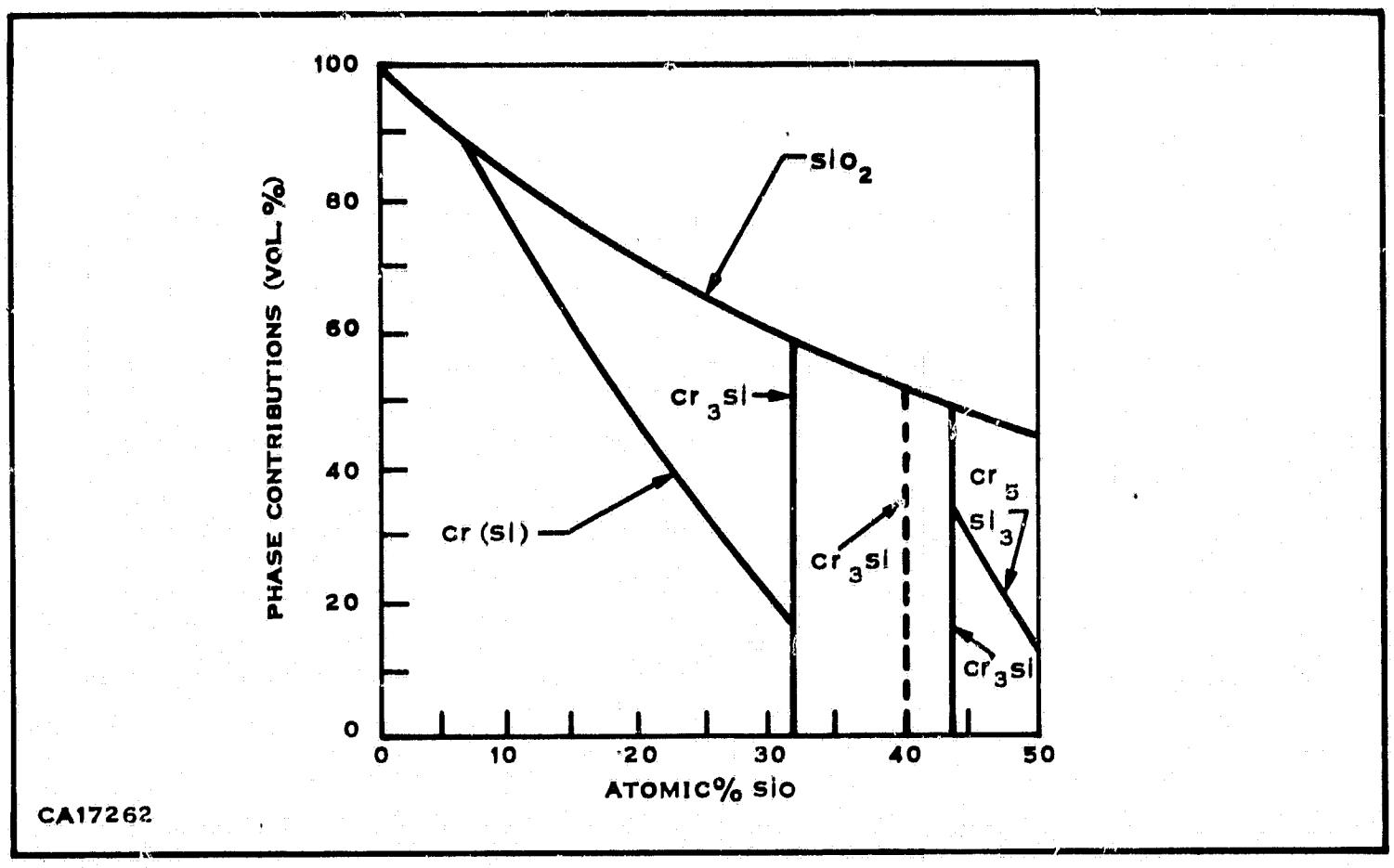


Figure 24. Cr-SiO Film Composition Diagram Assuming Complete Disproportionation of SiO and Reaction with Cr According to the Phase Diagram. Phase Volumes Calculated from Bulk Densities [20]

The properties of Cr_3Si have an important bearing on the interpretation of Cr-SiO cermet properties. Glang, et al. point out that Cr_3Si has a peculiar crystal structure in which the Si atoms form a bcc lattice with chains of Cr atoms parallel to the three crystal axes. The Cr atoms are packed closer than in pure Cr metal which is typical for the β-tungsten structure. The metallic character of the compound is indicated by a resistivity which is only about three times as high as that of Cr metal, and a positive TCR about twice as high as that of pure Cr. The higher order silicides exhibit decreasing metallic character in accord with the increased silicon content. For this reason as well as the increased presence of SiO_2, rising SiO concentrations should produce a trend of increasing film resistivities.

The dependence of film resistivity in micro-ohm-cm upon SiO content is plotted in Figure 20 for films as deposited at 200° C and after one hour vacuum annealing at 400°C, 500°C and 600°C. The results of other investigators are also included and will be discussed below. Glang, et al. claim that the resistivity of the pure Cr films (80–140 micro-ohm-cm) is due to the presence of a few percent Cr_2O_3, a previously observed phenomenon. The change in slope at 10 at % SiO is attributed to

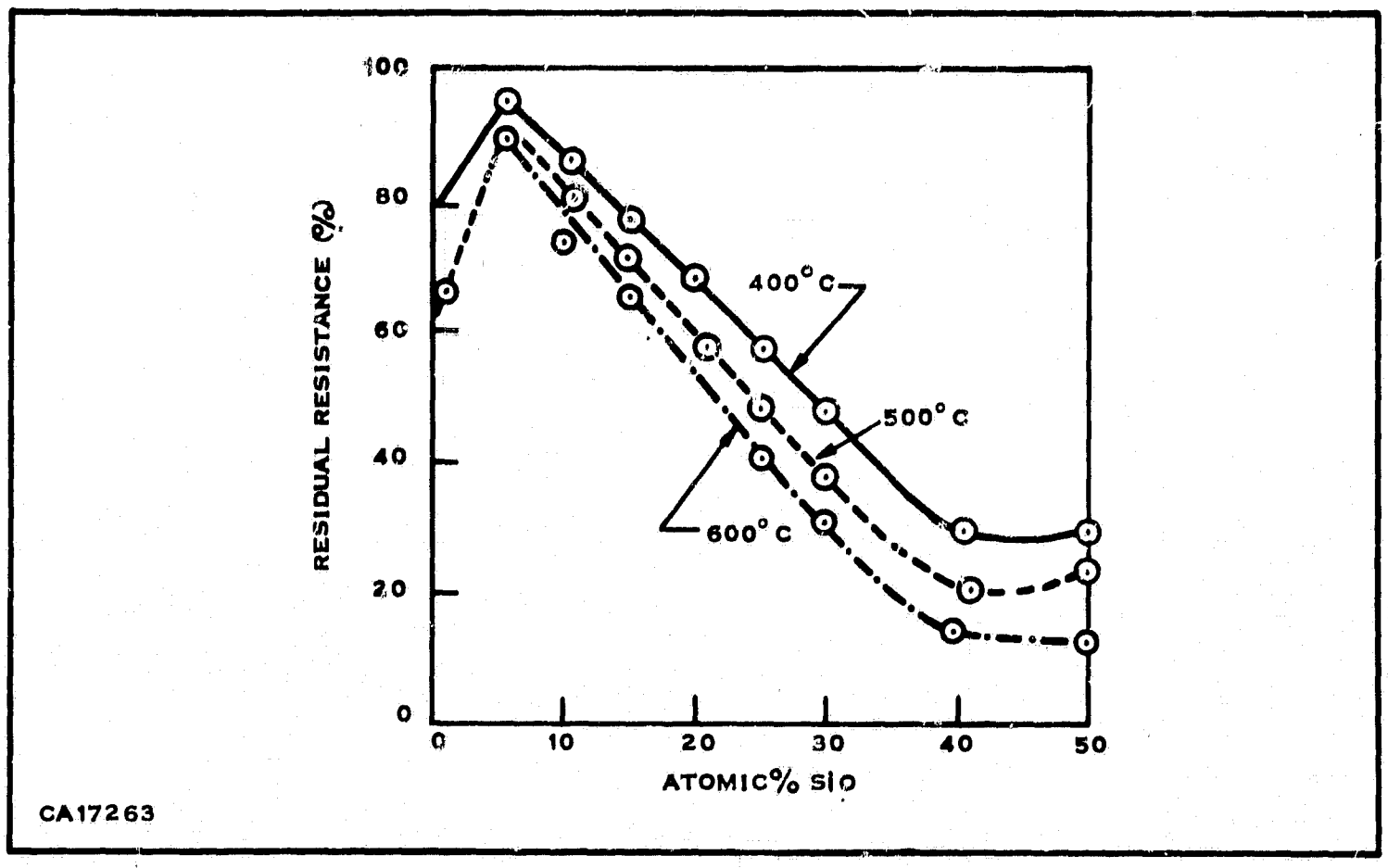


Figure 25. Residual Resistance of Cr-SiO Films After 1-h Annealing at Three Temperatures Versus SiO Concentration. One Hundred Percent Corresponds to the Initial State as Deposited at 200 Degrees C [20]

Cr_3Si formation by solid-state reaction rather than Cr diffusion. This argument appears reasonable in view of the presence of SiO_2 which impedes the metal diffusion process. Similar arguments were made by Beckerman and Thun (31) in regard to diffusion of gold in MgF_2 and SiO where in the latter case the lower atomic mobility of the dielectric resulted in smaller gold particles and considerably higher but less concentration-dependent resistivity. Thus, in the range 10% to 40% SiO part of the resistivity rise caused by SiO_2 is compensated by Cr_3Si formation. Above 40% SiO the slope increases due to formation of the more resistive silicide Cr_5Si_3. These films anneal to lower resistance values characteristic of the anneal temperature and independent of prior lower temperature thermal history. The fractional resistance reductions are a function of film composition as shown in Figure 25. If isothermal annealing for a constant time interval is employed, films of different composition but identical deposition temperature can be characterized by their resistance decrease (annealability). The regions of saturated resistance decrease are characteristic of onset of Cr_5Si_3 formation.

The regions of high Cr content where the Si is in solid solution show the smallest annealability, suggestive of minimal silicide formation. Similar conclusions may be derived from an examination of TCR versus composition dependence shown in Figure 21 where pre- and post-anneal curves are shown. Films deposited at 200°C prior to anneal all show negative values of TCR (25° to 85°C). Extended resistance measurements between −196°C and room temperature gave neither an exponential dependence on T^{-1} nor a strictly linear dependence on T, implying a combination of metallic and thermally activated conduction. As can be seen in Figure 21, annealing for one hour at 400°C generally results in TCR shifts to more positive values, the largest shifts occurring at higher SiO concentrations where silicide formation is most prominent. Glang, et al. attribute the chromium rich (<5 at % SiO) characteristics to thermally activated charge carrier creation and tunnelling through oxide barriers present in their films, which may be regarded as a metastable condition. Annealing tends to restore equilibrium conditions where disproportionation of SiO and subsequent dissolution of Si into Cr takes place, thus enhancing metallic conduction and positive TCR shift.

A different and more detailed explanation of the electrical behavior of Cr-SiO cermets in the composition range 0–10 at % SiO is offered by Lood (33). He considers the conduction processes from the point of view of band theory. Chromium apparently possesses two overlapping bands, one less than half full and one over half full. The positive contribution to the Hall coefficient R_H, from the latter predominates for pure chromium films. However, addition of SiO rapidly lowers R_H to negative values as seen in Figure 26. Lood suggests that a possible mechanism is that SiO introduces impurity levels that alter the electron populations in the bands, thus changing their effective masses, and hence, the sign of the Hall coefficient. The SiO levels could also account for a thermally activated carrier process resulting in increasingly negative values of TCR with increasing SiO content. In fact, from a knowledge of film resistivity dependence on SiO content, Figure 20 [which resembles Glang, Holmwood and Herd's (20) unannealed curve], Lood summed the TCR contribution from the chromium and the activated carriers assuming 1.0–1.5 electrons per SiO level and obtained a good fit to experimental TCR dependence on resistivity. It should be pointed out that Lood's films have significantly lower resistivity and more metallic TCR for SiO contents below 7 at % compared to Glang, Holmwood and Herd, who suspect Cr_2O_3 contamination in this range.

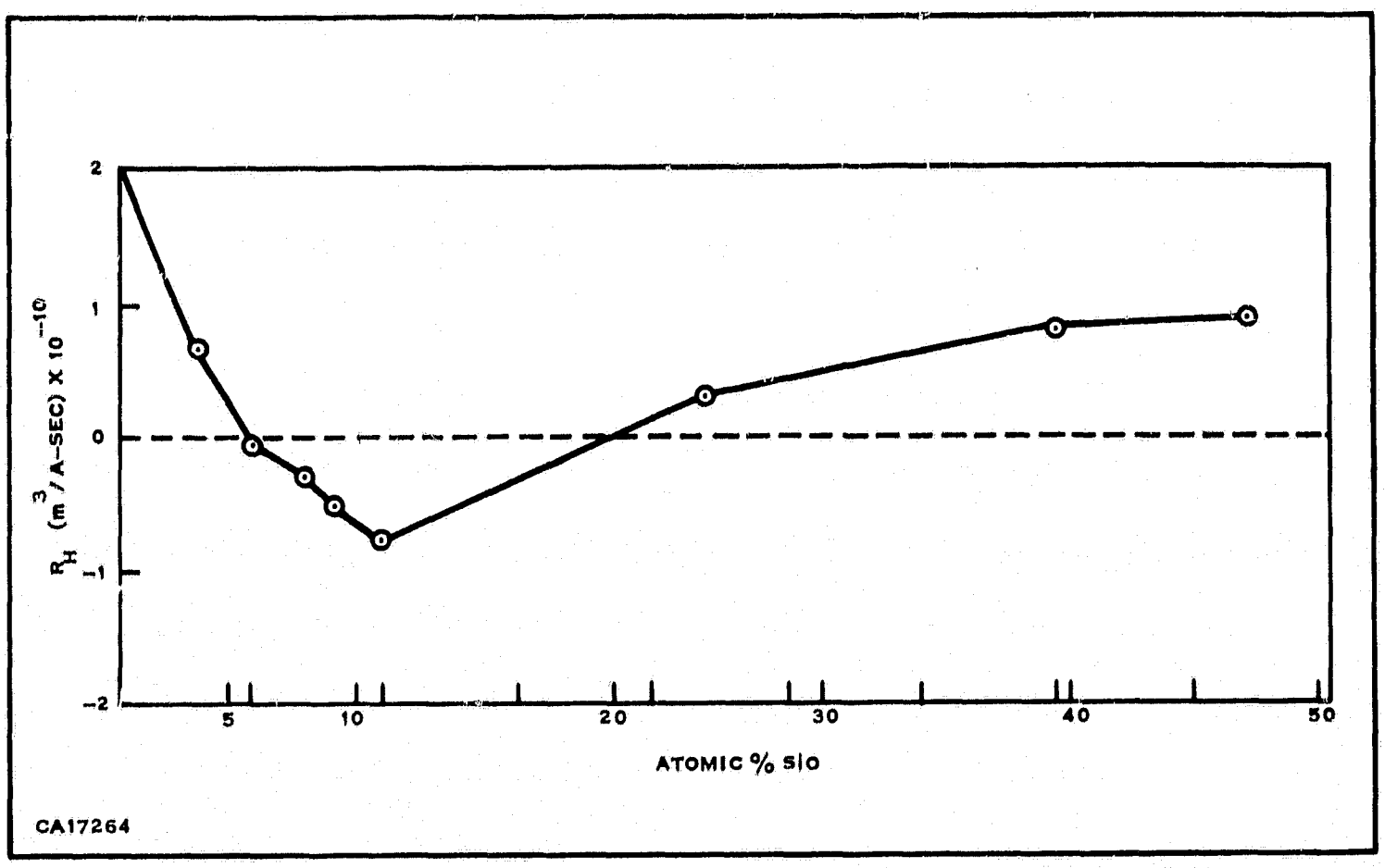


Figure 26. Hall Coefficient (25 Degrees C) as a Function of Film Composition [33]

Figure 20 also shows the resistivity versus composition dependence as observed by other workers mentioned earlier, together with data gathered under the reporting contract. In the only other flash evaporation study covered in this survey, Braun and Lood (29) examined a relatively narrow compositional range, approximately 26–53 at % SiO. Their films appear to be relatively unannealed compared to those of Glang, Holmwood and Herd. This is possible, since Braun and Lood only annealed to a desired resistance value which may have been insufficient to equilibrate the cermet. The limited TCR data follows the trend of the unannealed data of Glang, et al.

The data of Ostrander and Lewis (32) show excellent agreement with those presented so far, for SiO content below 25 atomic %. Between 25% and approximately 38 at % their values for resistivity are considerably higher. However, the TCR data shows conduction is metallic from 25 at % to 30 at % SiO before going negative. The authors have also shown that up to about 17 at % SiO the product TCR X resistivity is a constant, suggesting that the films are actually a homogeneous solid solution obeying Matthiesson's Rule for dilute solid solutions. It should also be pointed out that electron micrograph and diffractometer examinations indicate an amorphous system with occasional aggregates 100Å diameter whereas the micrographs of Glang, et al. (20), show considerably more structure. Ostrander and Lewis (32) do not indicate the

exact substrate deposition temperature. At least it was at or below 400° C for a period of four minutes during deposition. Cool down rate was unspecified so the degree of anneal is unknown. They indicate a two-hour anneal at 250° C (ambient unspecified) resulted in a resistance increase for all samples. It is probably safe to assume the samples were not annealed in the sense of Glang, et al.(20)

In view of the homogeneous nature of their films, the model Ostrander and Lewis used to analyze current transport appears reasonable. They assume an imperfect close packed lattice whose lattice sites are randomly occupied by either metal or insulator particles, uniform in size and spherical in shape. By calculating the minimum metal volume fraction permitting a contiguous structure of metallic spheres in two dimensions (the third dimension was ruled out because of preferred orientation normal to the surface), they obtained a coordination number of 3.5 below which Frenkel type conduction occurred. This approach is compatible with the rapid rise of film resistivity seen at higher SiO concentrations. It would be reasonable to suppose that a 400° C–600° C anneal for one hour would result in some silicide formation and possibly some metallic agglomeration, lowering the resistivity.

In comparison, the data of Beckerman and Thun (31) is entirely different, although they too used a coevaporation system. In their studies of Au-MgF_2, Au-SiO, Cr-MgF_2 and Cr-SiO, they obtained approximately exponential dependence of resistivity upon atomic SiO content for both Cr-SiO and Au-SiO systems, with Au-SiO exhibiting a somewhat smaller slope, due apparently to less tendency for the gold to recrystallize. The Au-MgF_2 and Cr-MgF_2 exhibit lower resistivities: $4.6\text{-}47 \times 10^{-6}$ and 5×10^{-5} – 1.3×10^{-3} ohm-cm, respectively, at high metal compositions, but the resistivity increases very rapidly when the dielectric content exceeds about 20 atomic %. This is similar to the behavior of Ostrander and Lewis' curve, although the presence of electron diffraction patterns in the Beckerman-Thun samples indicates significant grain structure. MgF_2 was found to inhibit metallic diffusion far less than SiO, which accounts for the larger particles and the sudden resistivity rise when contiguous contact ceases. The exponential resistivity dependence in the SiO containing chromium suggests a very fine dispersion of the metallic species; hence, current transport would be primarily by tunneling, the electron transmission probability depending exponentially on the width of the potential barrier impeding current flow. Electron micrograph data tends to confirm this supposition. In Cr-SiO cermets the metal grains were seen to be extremely small, less than 50Å in diameter. Beckerman and Thun further evaluated 70% Cr films fabricated by flash evaporation. It is not clear whether the negative range of TCR values obtained pertain to the coevaporated or the flash evaporated films.

An exponential dependence of resistivity on metal content was also obtained by Miller and Shirn (40) in co-sputtered films of Au-SiO_2, Cr-SiO_2, and Nichrome-SiO_2 with resistivity from 10^{-2} to 10^{8} ohm-cm. Transmission electron micrographs of their Au-SiO_2 cermets showed considerable structure, with a comparatively large discontinuous network of metal in the film. Dispersion does not seem as fine as in coevaporation. They also obtain an exponential dependence above 34 ohm-cm of resistivity with reciprocal temperature for Au-SiO_2, indicating a thermally activated conduction process. In the region 10^{-4} to 4 ohm-cm the resistance varies linearly with temperature. The authors (40) make reference to preliminary annealing experiments on Nichrome-SiO_2 films which show 6% resistance decrease and a negative shift in TCR at 300°C. From 350°—420°C resistance drops rapidly and TCR increases. Detailed annealing experiments on varying compositions should be very illuminating and may serve to reduce the difference in electrical properties between sputtered and evaporated films.

The properties of some other cermet systems besides Cr-SiO will be briefly discussed. The system Ta, Si, Cr, Al_2O_3 was investigated by Terry (28). Deposition was by powder flash evaporation using an E-gun source. Details concerning the mixture ratio were not given, although the constituents were felt to exist in the forms Cr_3Si, $TaSi_2$, Al_2O_3. Experiments involving increased quantities of Al_2O_3 resulted in higher resistivities. Sheet resistivities ranged from 100 to 10,000 ohms/square with corresponding TCR between +50 and −200 ppm/°C. The ρ versus TCR curve is very similar in shape to that for co-sputtered Au-SiO_2 and Nichrome-SiO_2 of Miller and Shirn (40).

Terry also examined some of the properties of Cr_3Si and $CrSi_2$ as deposited by the above method. The results are partially summarized in Table 4.

Note that, as expected, the TCR is positive, characteristic of metallic type conduction, also that the resistivity of Cr_3Si is lower than that of the higher silicide $CrSi_2$. Also, it has almost the same value as the annealed films of Glang, Holmwood and Herd (20) at the 15 atomic % SiO plateau where Cr_3Si formation occurs.

Included in the table on Cr-Si alloys is the data of Glang, Holmwood and Herd (20) which shows a slightly lower resistivity for Cr-17 at % Si, which is to be expected for a Cr-rich Cr_3Si solution. The data for as-deposited pure chromium is extracted from their plots. Apparently most deposited chromium films depart considerably from pure bulk values as is confirmed in the data of Lood (33) and Crossland, Rottgers (41). It should be noted that Crossland's close approach to bulk values

Table 4. Electrical Properties of Deposited CrSi Films

Worker	Evaporated Material	Rs (ohms/ square)	Thickness (Å)	Resistivity (micro-ohm-cm)	TCR (ppm/° C)	Remarks
Terry (28)	$CrSi_2$	100–200	400–500	500–1000	0 to +100	Powder flash evap.
Terry (28)	Cr_3Si	90–100	250–350	200–300	0 to +50	Ts* = 400°C
Glang, Holmwood	Cr–17% Si	–	–	182	+1	As deposited Ts = 200° C
+Herd (G, H, H)(20)	Cr–17% Si	–	–	163	+40	Annealed 400° C 1 hour
G, H, H (20)	Cr–17% Si	–	–	147	+70	Annealed 500° C 1 hour
G, H, H (20)	Cr–17% Si	–	–	129	–	Annealed 600° C 1 hour
G, H, H (20)	Cr	–	–	140	–80	As deposited Ts = 200° C
G, H, H (20)	Cr	–	–	100	+150	Annealed 400° C 1 hour
Lood (33)	Cr	–	–	40	+900	As deposited Ts = 200°C
Landolt Bornstein	Cr (bulk)	–	–	13	+3000	From Landolt-Bornstein
Crossland and Rottgers (41)	Cr	–	200–600	–	+1400 to +2100	Deposited by electron beam evaporation at 5×10^{-10} torr.

*Ts indicates the substrate temperature.

is due to having evaporated polycrystalline chromium at the low pressure of 5×10^{-10} torr. after extensive outgassing and precautions to avoide contamination.

4. Stability of Cermet Films

Schaible, Overmeyer and Glang (42) have shown that a primary source of instability in cermet resistors can be contact degradation, particularly under electrical as well as thermal stress. They observed that with dc load stress, high resistance regions developed under aluminum anode contacts, accounting for most of the resistance change.

Their measurements were performed on test resistors defined in 4-terminal configuration which permitted an estimate of the contact resistance. Although unspecified, the method of deposition is probably that of Glang, Holmwood and Herd (20). Figure 27 illustrates typical resistance behavior observed for the anode, cathode and resistor portions of a Cr–20% SiO resistor with aluminum contacts when stressed at elevated temperature and dc load. Onset of contact degeneration was accelerated by temperature and current stress, and is attributed to current induced mass transport of chromium from the cermet to the aluminum contact with which it reacts. This results in a metal-poor region in the vicinity of the contact which contributes the high contact resistance. That this is not just a temperature induced phenomenon can be seen from the fact that storage up to 200° C has no harmful side effects, whereas application of dc loads can result in contact increase at a temperature as low as 100° C.

The authors (42) have shown that the anodic resistance increase is directly related to the degree of reaction of the cermet metal species and the contact metal. By placing an inhibiting layer of chromium between Al and cermet, or by the choice of nonreacting metal contacts (Au or Cu), contact degradation was virtually eliminated. The results are summarized in Tables 5, 6, and 7. Table 5 demonstrates the superior stability of Cu contacts and the excellent cermet stability. Table 6 shows stability for different cermet compositions and anneal temperatures, while Table 7 shows stability for increasing stress load temperatures. Stability was excellent for temperature-load stresses up to 200° C and 20 mW/mil^2. Resistance changes were less than 1% for T<175° C, P = 40 mW/mil^2. At 80 mW/mil^2, resistance is seen to decrease at nearly all ambient temperatures; however, higher anneal temperatures are seen to result in improved stability.

Beckerman and Thun (31), who deposited a variety of cermet materials, including Cr-SiO, by controlled coevaporation of the constituents, reported stability under storage at 100° C and 200° C. Of the various cermet systems, Cr-SiO is

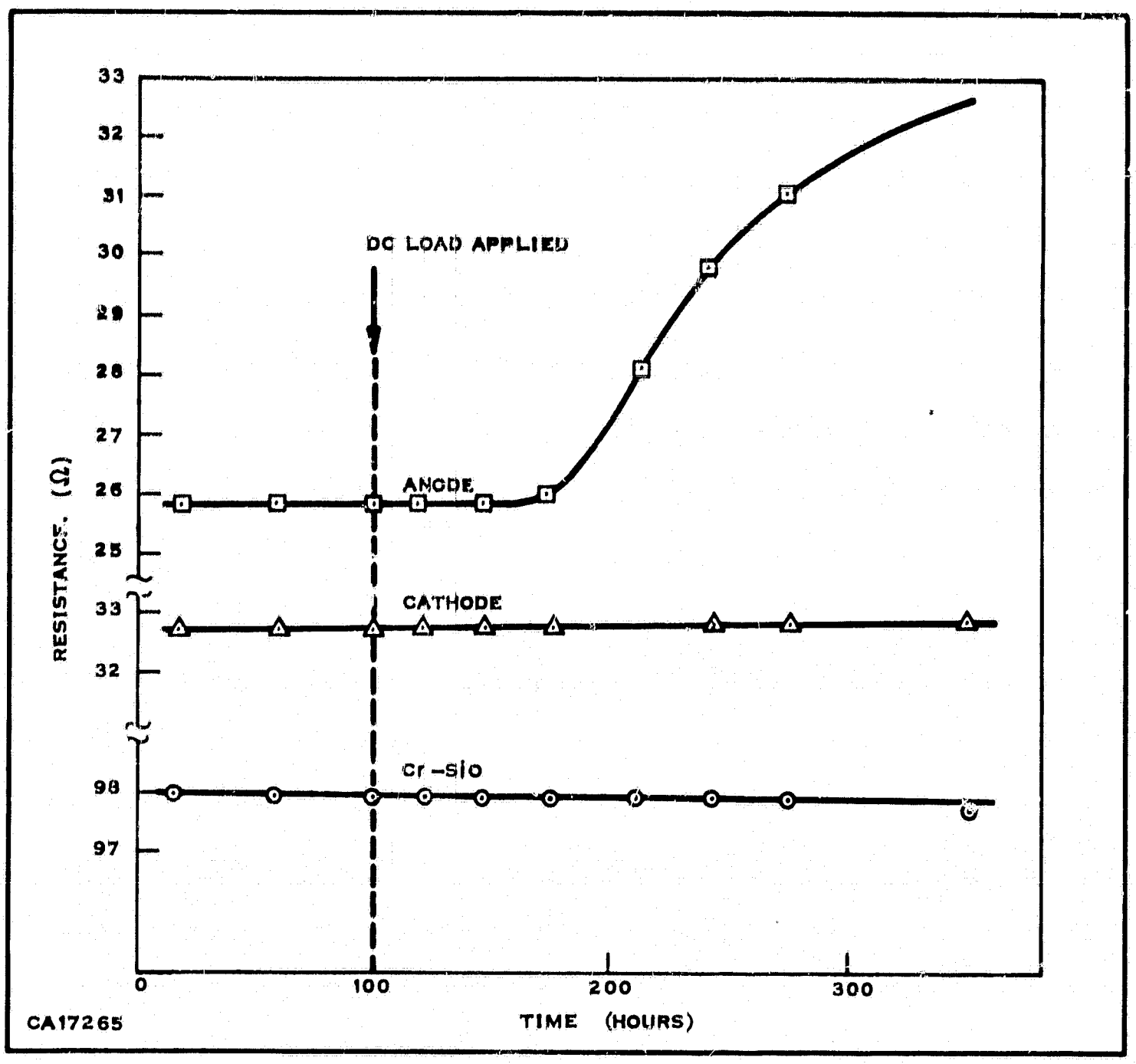


Figure 27. Resistance Versus Time Curves for Anode, Cathode and Cr-SiO Sections of Cermet Resistor with Al Terminals [42].

Table 5. Resistance Changes in Cr–20% SiO Resistors with Cu Terminals After 1000 Hours at 200°C and Various DC Loads. Stabilization Temperature = 400°C [42]

Power mW/mil^2	Ambient	Section	R_o Ohms	% Change
5	Argon	Cr-SiO	96	−0.04%
		Anode	31	−0.06%
		Cathode	28	−0.06%

Table 5. Resistance Changes in Cr-20% SiO Resistors with Cu Terminals After 1000 Hours at 200° C and Various DC Loads. Stabilization Temperature = 400° C (Continued)[42]

Power mW/mil^2	Ambient	Section	R_o Ohms	% Change
10	Argon	Cr-SiO	96	−0.03%
		Anode	31	−0.14%
		Cathode	28	−0.06%
20	Argon	Cr-SiO	96	−0.20%
		Anode	31	−0.09%
		Cathode	28	−0.22%
5	Air	Cr-SiO	105	+0.02%
		Anode	40	+0.02%
		Cathode	35	+0.04%
10	Air	Cr-SiO	105	+0.16%
		Anode	40	+0.19%
		Cathode	35	+0.80%
20	Air	Cr-SiO	105	+0.70%
		Anode	40	+0.40%
		Cathode	35	+0.30%

Table 6. Resistance Changes in Cr-SiO Resistors with Cu Terminals After 500 Hours at 200° C and 20 mW/mil^2 Load [42]

% SiO	Anneal Temp.	R_{Total} Ohms	Resistance Changes		
			Cr-SiO	Anode	Cathode
20	400°	182	−0.08%	−0.06%	−0.08%
30	400°	336	+0.05%	+0.21%	+0.04%
40	400°	568	−0.34%	−0.15%	−0.26%
50	400°	5090	−0.68%	−0.44%	−0.45%
20	500°	156	±0.01%	+1.8%	+1.0%
40	500°	424	+0.03%	+0.9%	±0.06%
50	500°	3760	+0.06%	−0.5%	±0.06%

Table 7. Stress Temperature—DC Load Matrix Showing % Resistance Changes of CR-20% SiO Resistors After 100 Hours [42]

Power mW/mil^2	Anneal Temp. °C	Stress Temp. °C				
		25°	100°	150°	175°	200°
5	400°			±0.01%	±0.01%	±0.01%
10	400°			±0.01%	±0.01%	±0.01%
20	400°			±0.01%	±0.01%	−0.02%
40	450°		±0.01%			
40	400°	±0.03%	±0.01%		−0.8%	
80	500°		−0.1%		−0.7%	
80	450°		−0.1%		−2.0%	
80	400°	±0.01%	−0.8%		−8.5%	

unquestionably the most stable. Results are summarized in Table 8. They have also studied the Cr-SiO system further by flash evaporating 70% Cr films and subjecting these to 42 temperature-humidity cycles. The resistors were found to be stable to 0.2%. It should be pointed out that the load level applied (<11 W/in.^{2}) was quite low compared with the stresses applied by Schaible, et al. (42) (1W/in.^{2} = 10^{-3} mW/mil^2).

Table 8. Percentage Change in Resistance of Cermets Under Various Conditions [31]

Cermet	% Change at 100° C for 200 hr	% Change at 200° C for 200 hr	% Change at 4 W in.^{2} 100° C for 100 hr	Temperature Coefficient of Resistance (ppm)
Au-MgF_2	–	–	3%	+600
Au-SiO	8%	20%	–	−2000 to −3000
Cr-MgF_2	<5%	<5%	–	–
Cr-SiO	<1%	<1%	–	−50 to −200

Flash evaporated Cr-SiO cermets were also evaluated for stability by Braun and Lood (29). Their results show uniform drift in the direction of increasing resistance of approximately 1 percent per 1000 hours for storage at 200°C, and 0.25 percent per 1000 hours for storage at 150°C. This is thought to be due to oxidation of the chromium. Good resistance to moisture was also observed. Unprotected resistors directly exposed to 60°C, 95% relative humidity showed no significant changes after 500 hours.

Cermets fabricated by evaporation of a mixture of Cr-SiO were examined by Pitt (30) for stability under electrical, thermal and humidity stress. His results are quoted verbatim below.

> Long-term life tests
>
> The results of these sequences of life tests on cermet resistors at various sheet resistances are shown in Figure 28. For comparison one Nichrome result is also given. The four tests are summarized in Table 9.
>
> On load very little drift occurred in 2,000-ohms/sq. resistors; the mean drift of test 1 at 5,000 h was $\pm$0.03%, the comparative NiCr figure being +0.18%. A similar test on 300 Ω resistors gave a mean drift of −0.07% in the same period. During the 5,000 h of both tests the largest mean drifts were −0.08% and +0.04%. The maximum negative drift of any sample was −0.10% but 3 resistors showed, from the first measurement, positive drifts relative to the remainder. These were later found to be anomalously noisy and to have some substrate damage in the vicinity of the resistor track. Their maximum drift in 5,000 h was +1.25%.
>
> A storage test at 100°C on 1,250-ohms/sq. samples gave a mean drift of +0.17% at 5,000 h and a maximum individual drift of 0.30%. No "rogues" were found during shelf tests. Low sheet resistance cermet shows much greater mean drift than the high-sheet-resistance material, +0.18% in 5,000 h compared with +0.25% for evaporated Nichrome. The process was optimized for the stabilization of high value cermets and a different ageing cycle from that used for higher values may improve the stability. However, there were no anomalous drifts and no resistors had noise values greater than 0.14 μV/V and there was no correlation between noise and drift.

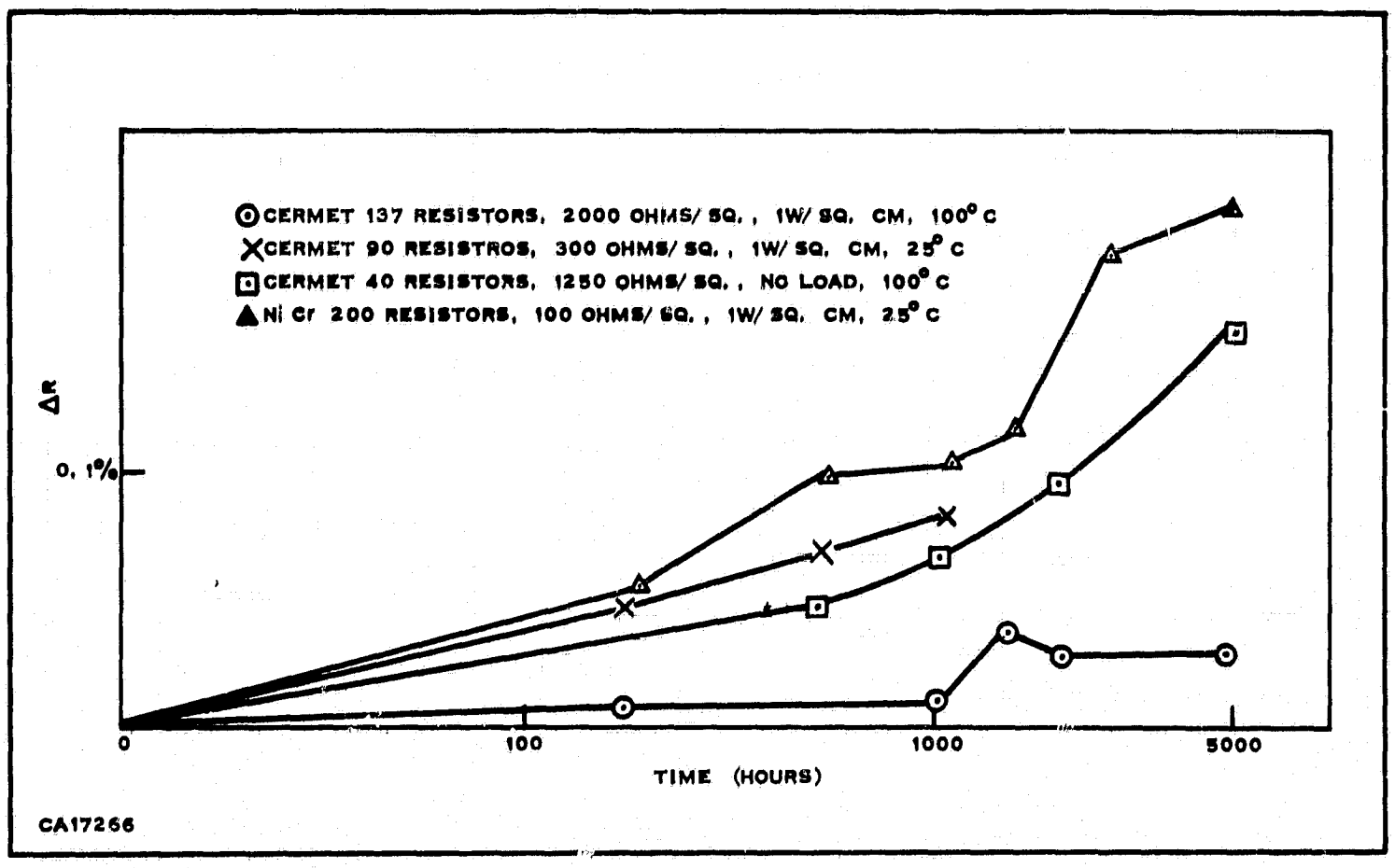


Figure 28. Life Test Results [30]

Table 9. Summary of Life Test on Cermet Resistors [30]

1	CrSiO	2,000 ohms/sq.	137 resistors	1 W/sq. cm	100°C
2	CrSiO	1,250 ohms/sq.	40 resistors	no load	100°C
3	CrSiO	300 ohms/sq.	90 resistors	1 W/sq. cm	25°C
4	NiCr (evaporated)	100 ohms/sq.	200 resistors	1 W/sq. cm	25°C

5. Reproducibility of Cermet Films

Glang, Holmwood and Maissel (34) have pointed out the dependence of annealing behavior on composition; thus the effect of resistivity fluctuations on film uniformity is in many instances enhanced after anneal. Their technique of flash evaporation appears to not only yield excellent compositional and monitor correlation, but also to afford superior reproducibility from wafer-to-wafer and run-to-run. They performed three test runs of 6 wafers each for a series of pellet compositions. The resulting deviation from the mean is shown in Table (10). Greatest uniformity is seen in the composition range 10-30 mole % SiO. The higher SiO compositions show poor

Table 10. Scattering Limits of Cermet Film Sheet Resistances After Annealing [34]

Pellet Composition (mole % SiO)	± Max. Sheet Resistance Deviation (%) After Annealing at 400° C			
	Run 1	Run 2	Run 3	From Common Average of Three Runs
0	3.4	9.5	1.8	9.1
5	5.7	2.3	2.1	7.0
10	1.0	2.1	2.0	3.3
15	1.3	1.2	1.6	2.6
20	1.7	0.6	2.2	2.3
25	1.0	1.0	0.9	2.9
30	1.0	0.9	1.2	3.7
40	1.5	3.6	3.4	5.1
50	4.4	4.6	3.5	12.0

run-to-run reproducibility, and fair uniformity within each run. Chromium rich deposits containing less than 10% SiO are neither very reproducible nor reliably uniform. Nevertheless, the pellet flash evaporation technique, as described, holds great promise for the controllable production of uniform cermet films.

The flash evaporation technique was also evaluated for reproducibility behavior by Braun and Lood (29). Note however, that this is a powder, not a pellet technique and is prone to compositional variations (see Section III A-2c this report). With nominal resistivities of 10^{-3} ohm-cm, Braun and Lood claim resistivity reproducibility of ±10%, with sheet resistance control to ±5%. Control deteriorates with higher SiO content. With nominal resistivities of 3.5×10^{-3} ohm-cm, control of resistivity was limited to ±20%.

In the fabrication of integrated circuit resistors, 1-mil wide, Braun and Lood found that: the average deviation in adjacent units was ±0.6%, and for 0.5 mil wide resistors, ±1.1%. For non-adjacent resistors on a 0.060" square chip, the deviations averaged ±1.8% for 1-mil wide resistors and ±2.5% for resistors 0.5 mil wide. Increasing the width beyond 1 mil afforded only slight improvement. With regard to absolute values, Braun and Lood claim their 1-mil resistors normally fall

within ±15% of the design value. They attribute about half of this deviation to resistivity and thickness variations. The remaining variance is due to variations in dimensions arising from processing fluctuations. Fig. (18) shows a typical distribution of 1-mil wide cermet resistors on a 1-inch diamter silicon substrate, and a comparison with distributions attainable for diffused resistors.

No detailed information has been seen on reproducibility data for co-evaporated cermet resistors. Beckerman and Thun claim sheet resistivity reproducibility of ±2.0 %.

A control problem experienced in cermets deposited by evaporation from a mixture of Cr and SiO was discussed in some detail by Pitt (30) and is reproduced verbatim:

> The scatter in Fig. 29 is due to a combination of scatter within and between batches. Earlier experiments at 2,000 - 3,000 ohms/sq. gave a mean reproducibility of ±20%. In the more recent results reported here this has been improved to ±12% but compares unfavourably with ±5% at 200 ohms/sq. The scatter of individual resistor properties within a batch is not only confined to random fluctuations of value, it also appears as a wide range of temperature coefficients and as anomalously high noise values. At 200 and 300 ohms/sq. there are no resistors with properties sufficiently different from the majority to classify them as potential "rogues". At higher sheet resistances the incidence of "rogues" as indicated by noise and lift tests figures may be as high as 2-4%.

Finally, in the only reference cited here on sputtered cermet films, Miller and Shirn (40) claim resistance uniformity of ±10% for stainless steel - SiO compositions. This corresponds to ±0.2% in metal weight percent, and was considered by the authors as very satisfactory.

B. EXPERIMENTAL: MASS SPECTROMETRIC DETERMINATION OF THE VAPOR SPECIES ABOVE A HEATED MIXTURE OF SiO-Cr.

The simultaneous evaporation of two components to form cermet film resistors can be conveniently studied by means of a mass spectrometer. Since the composition of the vapor and the changes it undergoes with time is important in understanding the processes occurring in such an evaporation, a mass spectrometric approach was used

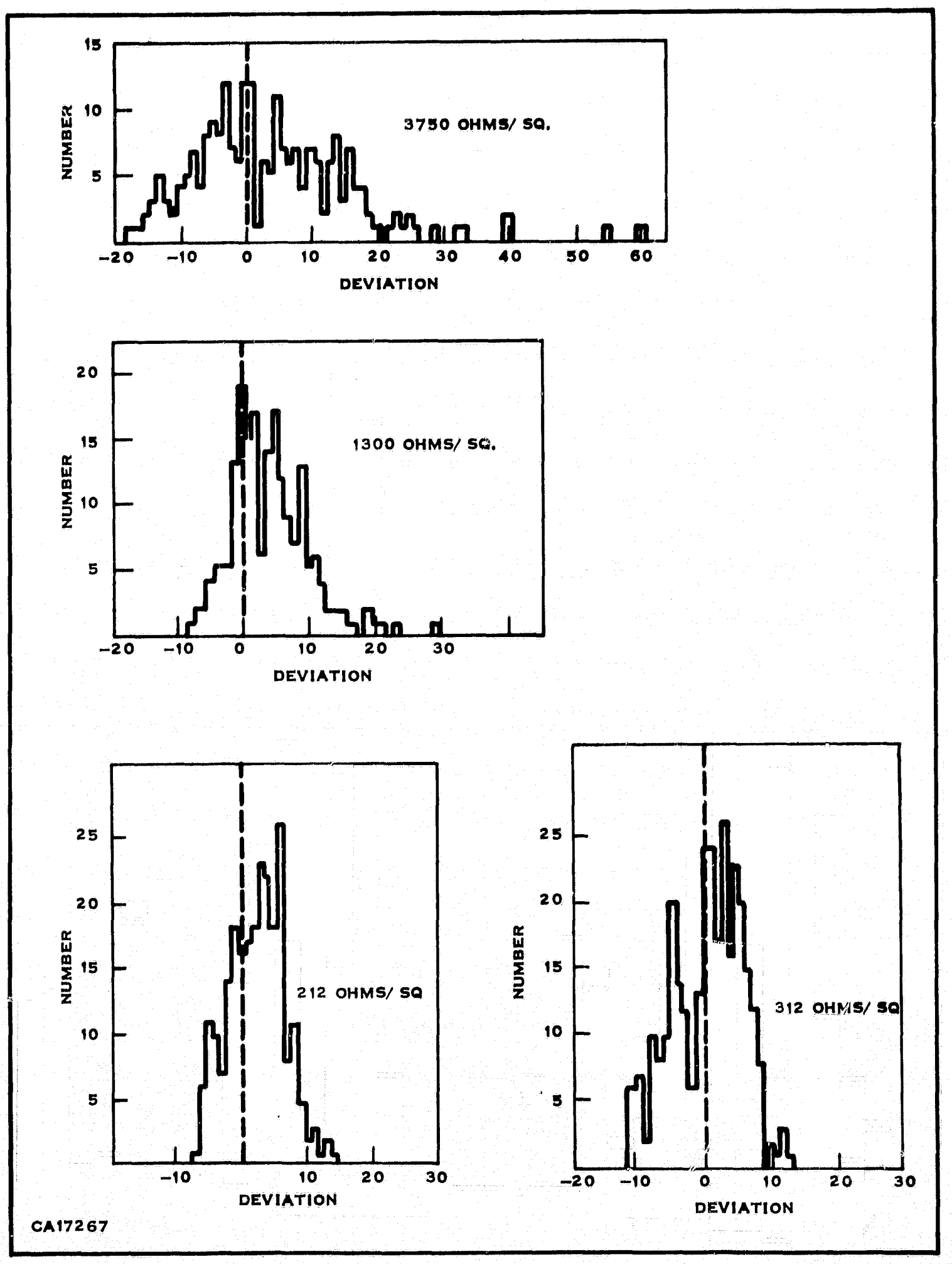


Figure 29. Histograms of Resistor Deviations from Target Value for Four Different Sheet Resistivities [30]

under this contract in an effort to elucidate some of the following problems. What is the composition of the vapor? Does the composition change with time? How important is the temperature: Can a charge be used for more than one evaporation?

A small (unweighed) mixture of SiO (25% by weight) and Cr (75% by weight) powder was placed on a tantalum filament with a heated area 5 mm by 10 mm. The filament was cleaned by heating to 1500°C in a high vacuum. Two large stainless steel poles supporting the filament were mounted on a water cooled base plate. This assembly was inserted directly below the ionization chamber of a Bendix time-of-flight mass spectrometer. The spectrometer was then pumped down to about 5×10^{-7} mm of Hg by using two ion pumps. All spectra were taken with 70 ev electrons.

The filament was heated resistively with an ac power supply. Temperatures were measured with an optical pyrometer, viewing through a glass port and a mirror. No corrections were made for the glass or for the emissivity of the tantalum filament. In a typical experiment the filament was taken to its final temperature rapidly, followed immediately by consecutive scans every 15 seconds for a total of 15 minutes. Continuous visual observation of the mass spectra was also possible during a run by use of an oscilloscope. The total pressure in the system was never higher than 10^{-5} mm of Hg.

The results for three temperature runs, 1110°, 1215°, and 1310°C are shown in Figures 30—32. These plots are actually ratios of the peak intensity of a particular ion divided by the peak intensity of argon. Argon is present in the mass spectrometer as background due to a small air leak. Since its ion intensity should remain constant during an experiment, its intensity was used as a reference to compensate for possible fluctuations in ion source conditions.

It should be pointed out that these ion intensities are not absolute or quantitative. In order to obtain quantitative information the ionization and detection efficiencies of SiO and Cr would have to be taken into account. Since the masses of SiO^+ and Cr^+ are approximately the same, it is assumed that their detection efficiencies are equal. Therefore, quantitative variations in the measured ion currents of the two species should be the result of differences in ionization cross-sections of the two molecules. The ionization cross-sections for SiO and Cr were obtained from the work of Otvos and Stevenson (43), and yield a ratio of Cr/SiO = 1.6. The SiO^+ curves could be multiplied by this factor, but possible errors in the temperature measurements in

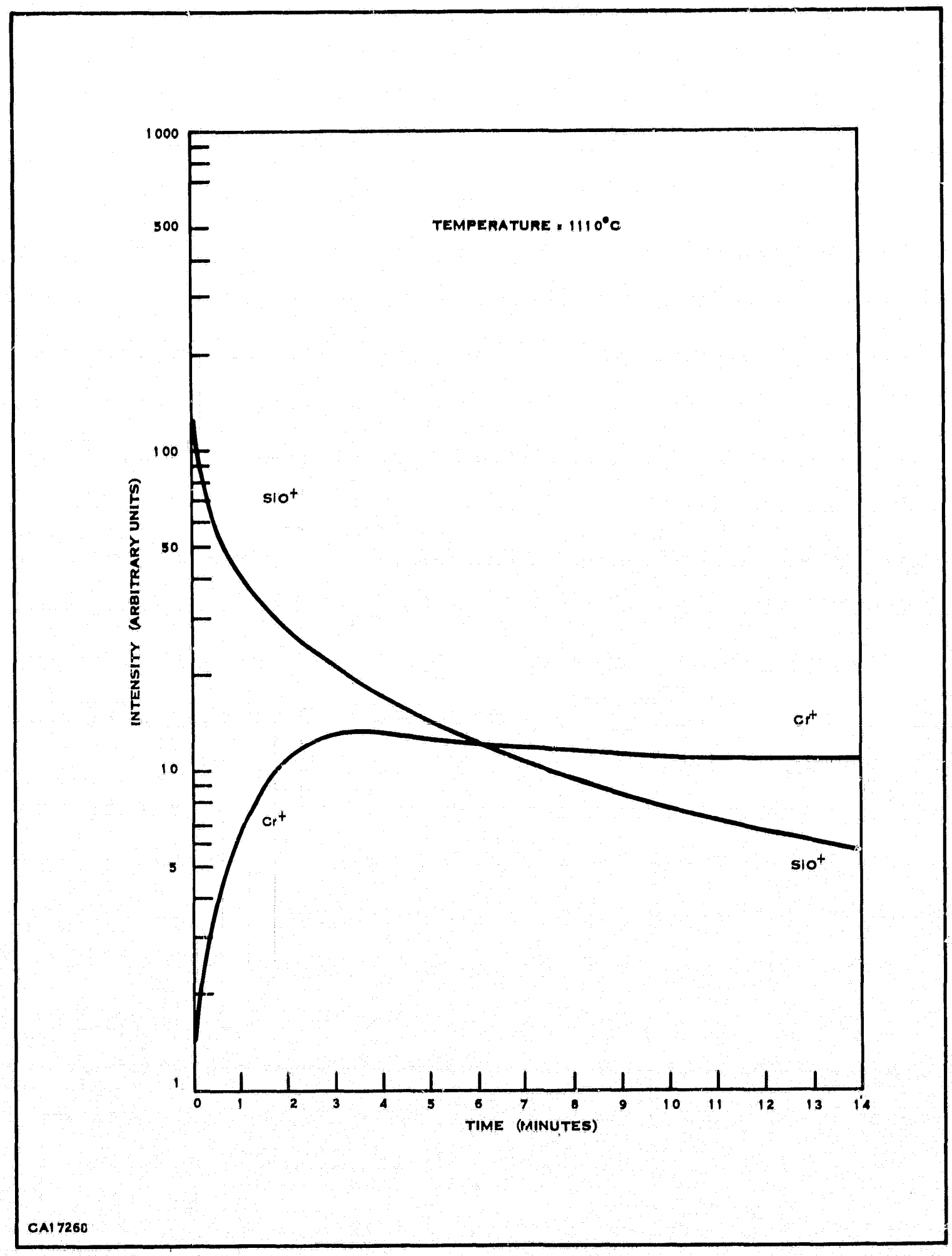


Figure 30. The SiO^+ and Cr^+ Ion Intensities Versus Time at 1110 Degrees C

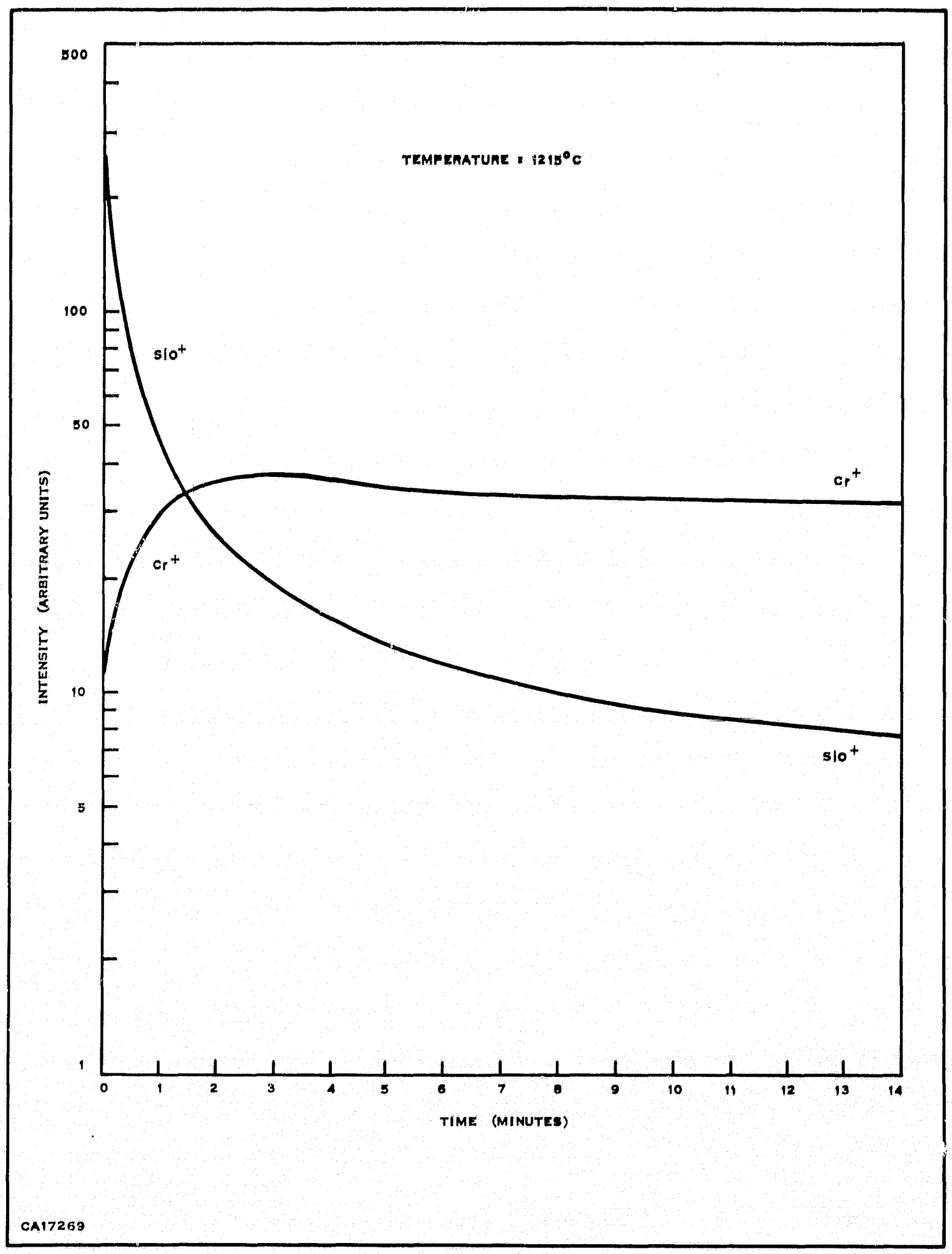


Figure 31. The SiO and Cr Ion Intensities Versus Time at 1215 Degrees C

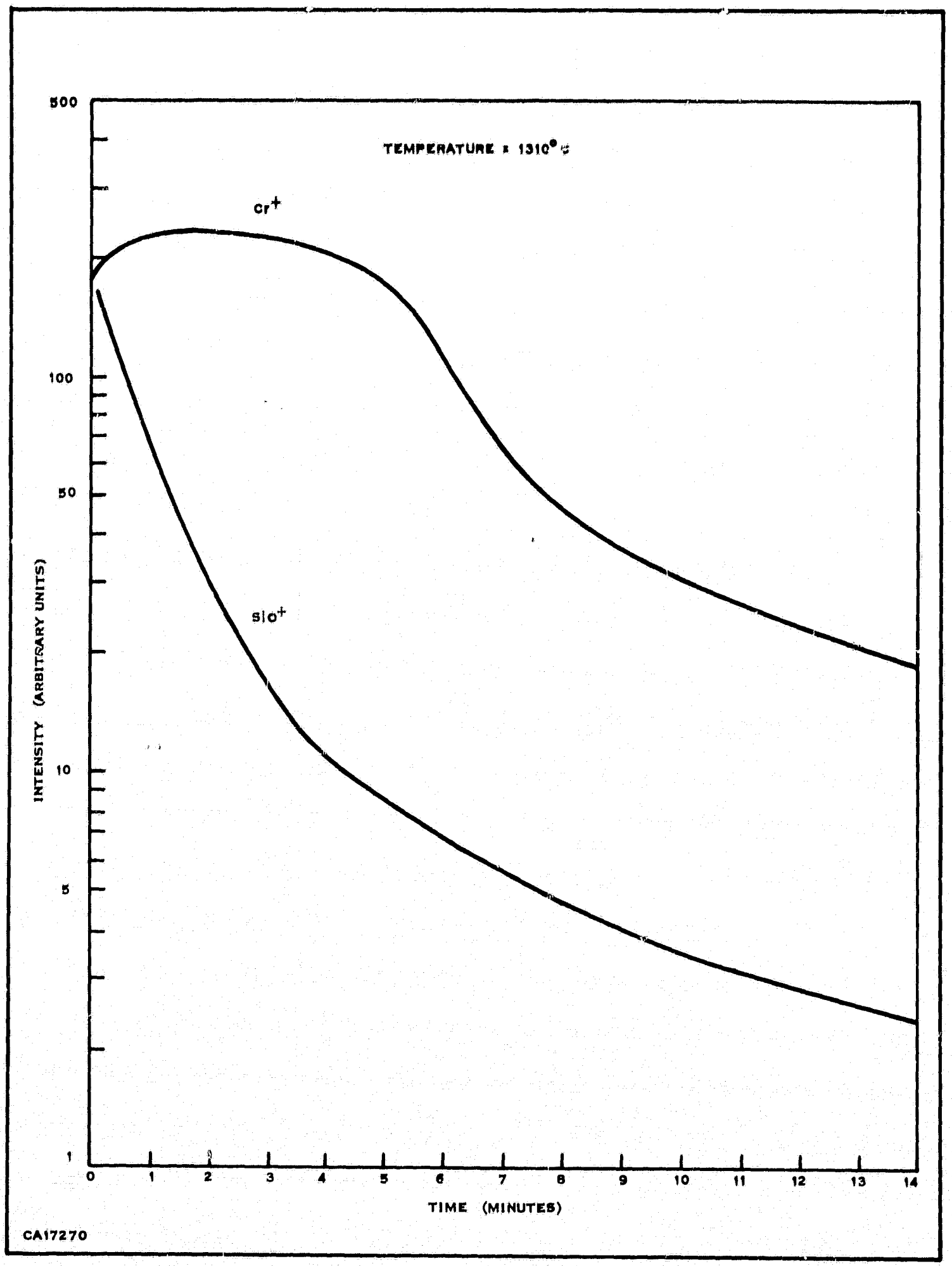


Figure 32. The SiO and Cr^+ Ion Intensities Versus Time at 1310 Degrees C

addition to the assumptions concerning the ion currents stated previously do not justify making this small correction. Also, no attempt was made to calibrate the mass spectrometer for SiO and Cr mixtures. Nevertheless, significant information can be derived from the results by considering the relative changes the SiO^+ and Cr^+ ions undergo at a given temperature with respect to time.

In Figure 30 it can be seen that there is considerably more SiO present in the gas phase than Cr at the beginning of the heating process of the 1110° C run. Large changes occur in the first three minutes of heating, namely the vapor pressure of SiO is high enough (approximately 0.1 mm of Hg) (44) that rapid depletion of this species from the sample takes place, while the Cr intensity increases then levels off. This initial increase in Cr is due to the time required to bring the metal up to its final temperature. After this temperature is obtained, the Cr^+ ion current levels off and remains at this value until depletion of the Cr. It is obvious that the composition of the vapor undergoes significant changes with time. These changes could seriously affect the outcome of the vaporization process and the final products.

One of the questions concerning the evaporization process was whether or not a charge could be used more than once. The problems encountered in this area can be explained by noting that the vapor phase composition is continually changing over a period of several minutes; depending on the size of the charge, while Cr is being vaporized at a constant rate, SiO is slowly disappearing. This would mean that subsequent evaporations with the same charge would probably require different deposition times for making the same value resistors.

The temperature run at 1215°C is similar in form to the 1110° C run. The SiO^+ curve in Figure 31 is almost identical to the one at the lower temperature, but the big difference is the Cr^+ curve. The Cr vapor pressure has increased with respect to the SiO vapor pressure. Obviously, the vapor pressure of SiO has also increased, but at this temperature its vapor pressure is so high (approximately 1.0 mm of Hg) (44) that most of the SiO has been vaporized and pumped away. Large increases in pressure were observed when the filament was turned on, then decreased rapidly before the first scan could be taken. This pressure increase was probably due to the large amount of SiO being vaporized.

To further illustrate the temperature effect, a run at 1310°C is shown in Figure 32. Another increase in the Cr^+ ion current with respect to that of the SiO^+ ion is observed.

Also, at this temperature the Cr metal is heated very rapidly, attains a maximum intensity as before, then begins to decrease. This decrease is a result of the depletion of the Cr metal from the charge, and parallels the SiO^+ ion curve throughout the remainder of the time study.

Since absolute ion intensities for each species are not known and sample charges were not weighed, a comparison between the temperature runs can only be made by examination of the SiO^+ to Cr^+ ion intensity ratios. These results are plotted in Figure 31. The somewhat irregular behavior of the 1310° C curve is due again to the depletion of Cr metal.

Some additional information was obtained from this study which is considered to be important in the elucidation of the overall evaporation process. Allam, et al. (45) have concluded that Cr_3Si is formed in the evaporation source, and further, that Cr_3Si is volatile. An exhaustive search of vapors from several charges in the mass spectrometer over a temperature range from room temperature to approximately 1500° C revealed no species other than Cr^+, SiO^+, Si^+ and O^+. The latter two species are due to fragmentation and ionization of the SiO molecule in the mass spectrometer. If a species such as Cr_3Si had been formed in the vapor phase, its mass spectrum could have readily been identified.

It has been suggested by Glang, et al. (20) that Cr_2O_3 can be formed in a SiO-Cr system. This green oxide was found to cover the outer surface of charges which had been heated in the mass spectrometer. The appearance of this oxide is not due to a reaction(s) with either SiO, SiO_2, or any product from the disproportionation of SiO, since samples of Cr heated in the mass spectrometer without SiO present also produced surface oxidation. Therefore, the oxide must be formed either from the reaction of the hot Cr metal with the oxygen present in the spectrometer from the small air leak, or from oxygen which is adsorbed on the surfaces of the filament, Cr powder, and filament support posts. When these components are heated, this adsorbed oxygen could be released, creating an increased supply of O_2 in the vicinity of the hot metal. The latter choice is more feasible since the mean free path of O_2 at the operating pressures of 10^{-5} to 10^{-6} mm of Hg is quite large (approximately 160 feet).

In summary, the vapor phase above a mixture of SiO and Cr consists of only these two species. Cr_3Si or related species were not observed. The amount of each species in the vapor phase varies with both time and temperature.

Three considerations prevent a direct application of the mass spectrographic data to the detailed analysis of structural composition of Cr-SiO cermet films deposited by filamentary evaporation of the mixture. They are:

1) Lack of quantitative relationship between the ion species and vapor phase constituents.
2) Lack of information concerning the detailed shape of the initial portions of the Cr and SiO deposition rate curves.
3) Lack of knowledge of the exact effective charge temperature.

If we make some simplifying assumptions, yet recognizing the validity of the above restrictions, we may nevertheless proceed to utilize the above mass spectrometer data. We assume:

1) The mass spectrometer ion intensity is directly proportional to the vapor phase flux. The proportionality constant is the same for chromium and SiO.
2) The SiO^+ and Cr^+ ion intensity data at short times is extrapolated to zero time as shown.
3) The effective charge temperature is the arithmetic mean of the top and bottom filament temperatures.

With these assumptions, we may proceed to calculate the flux integral with time and plot this against time. This is shown in Figure 34 for $T = 1215^\circ C$. N_s is the integrated SiO flux in arbitrary units, N_c is the chromium flux. The ratio $R = N_s/N_c$ is also plotted. We now observe the apparent change in overall film composition with deposition time. Furthermore, we can estimate the shape of the N_s/N_c curve if the shutter is closed in the first minute of deposition. This is also plotted in Figure 34 and is seen to result in a very different set of curves. A similar set of curves for $T = 1310^\circ C$ is plotted in Figure 35. With a knowledge of the compositional ratio R we may also estimate the cumulative atomic fraction of either constituent of the deposited mixture. Thus, we have the atomic percent content of SiO in the film = $F = (100\ N_s)/(N_s + N_c) = (100\ R)/(R + 1)$. This is plotted in Figure 36 for all the conditions in Figures 34 and 35.

It is also useful to plot the atomic percent SiO fraction, f, of the depositing cermet. If we denote $SiO^+/Cr^+ = (dN_s/dt)/(dN_c/dt)$, then $f = (dN_s/dt)/(dN_s/dt + dN_c/dt)$. Values of f are calculated from Figure 33 and plotted in Figure 37. The above curves will be used in later Sections (III.F.1-6) in discussions on film composition.

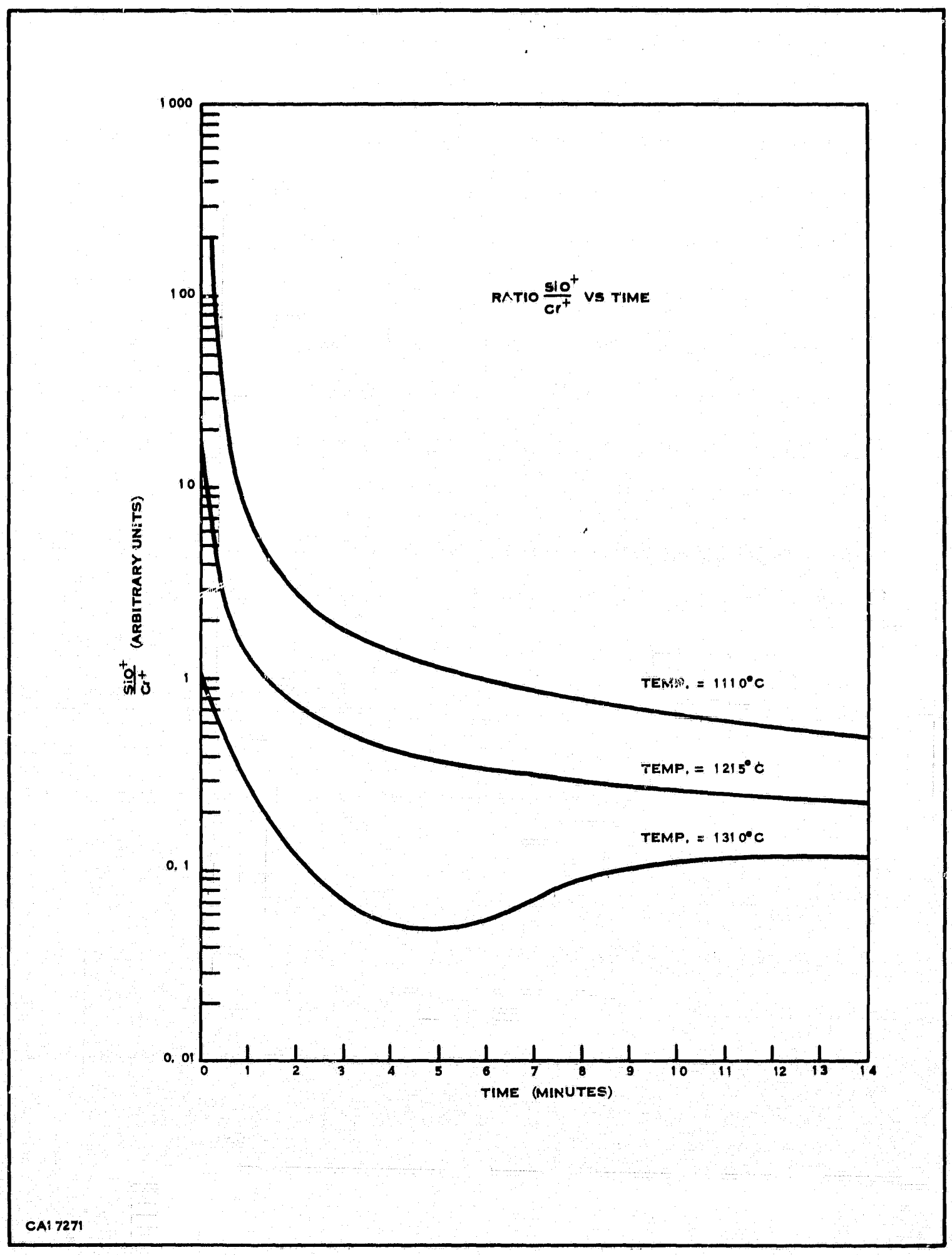


Figure 33. The Ratio of the SiO^+ Ion Intensity to the Cr^+ Ion Intensity Versus Time at 1110 Degrees, 1215 Degrees, and 1310 Degrees C

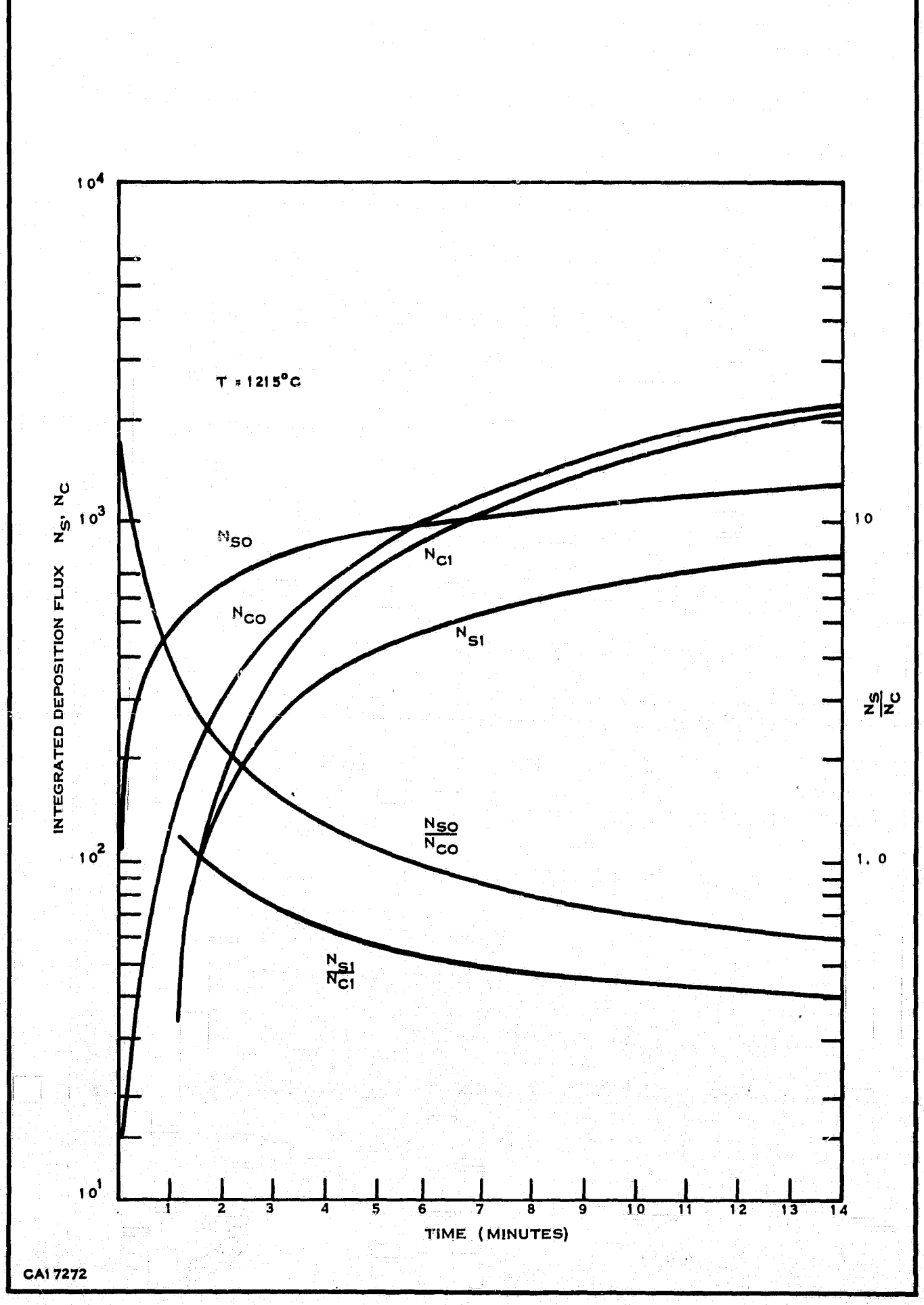


Figure 34. Variation of Integrated Deposition Flux with Time T Equals 1215 Degrees

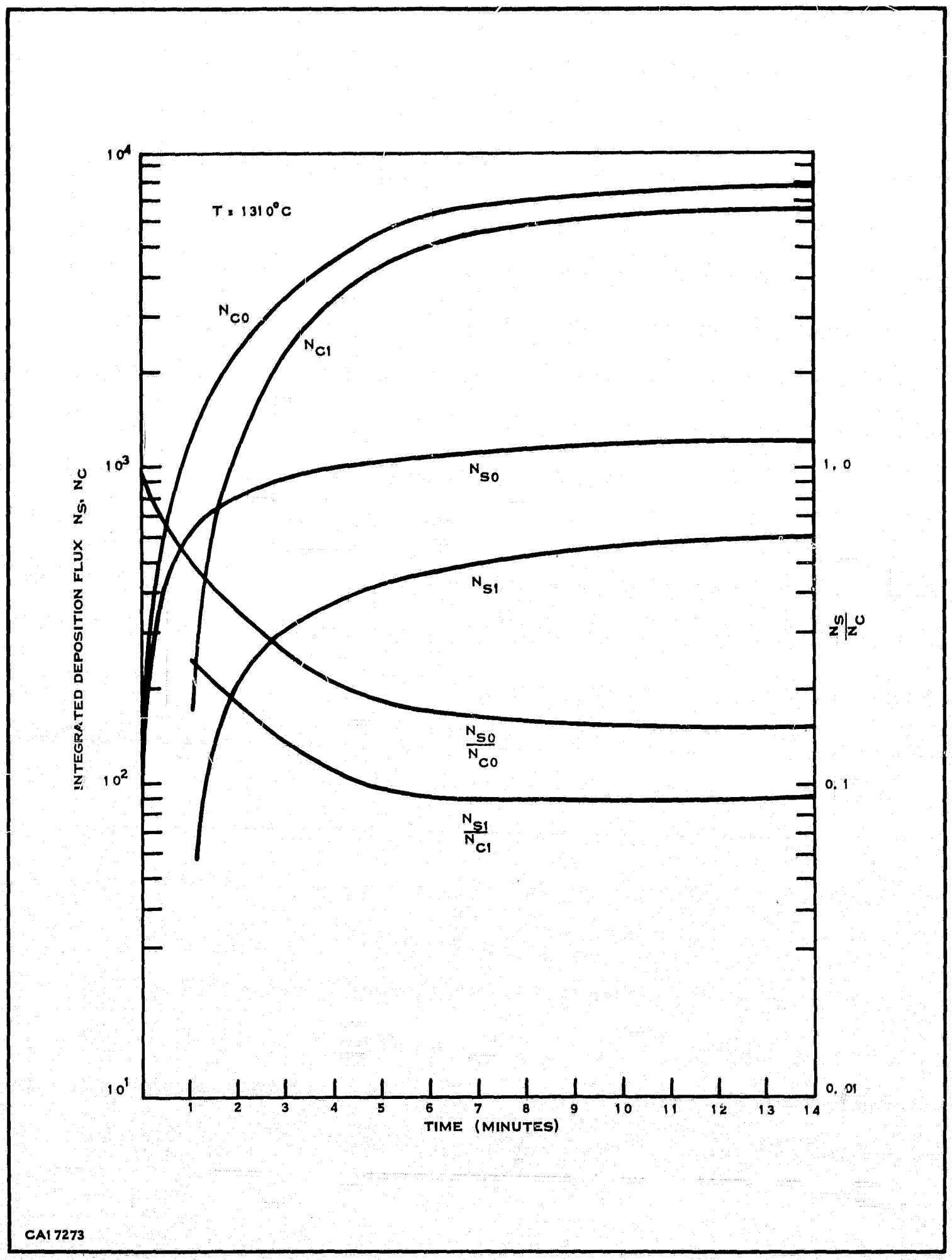


Figure 35. Variation of Integrated Deposition Flux with Time
T Equals 1310 Degrees C

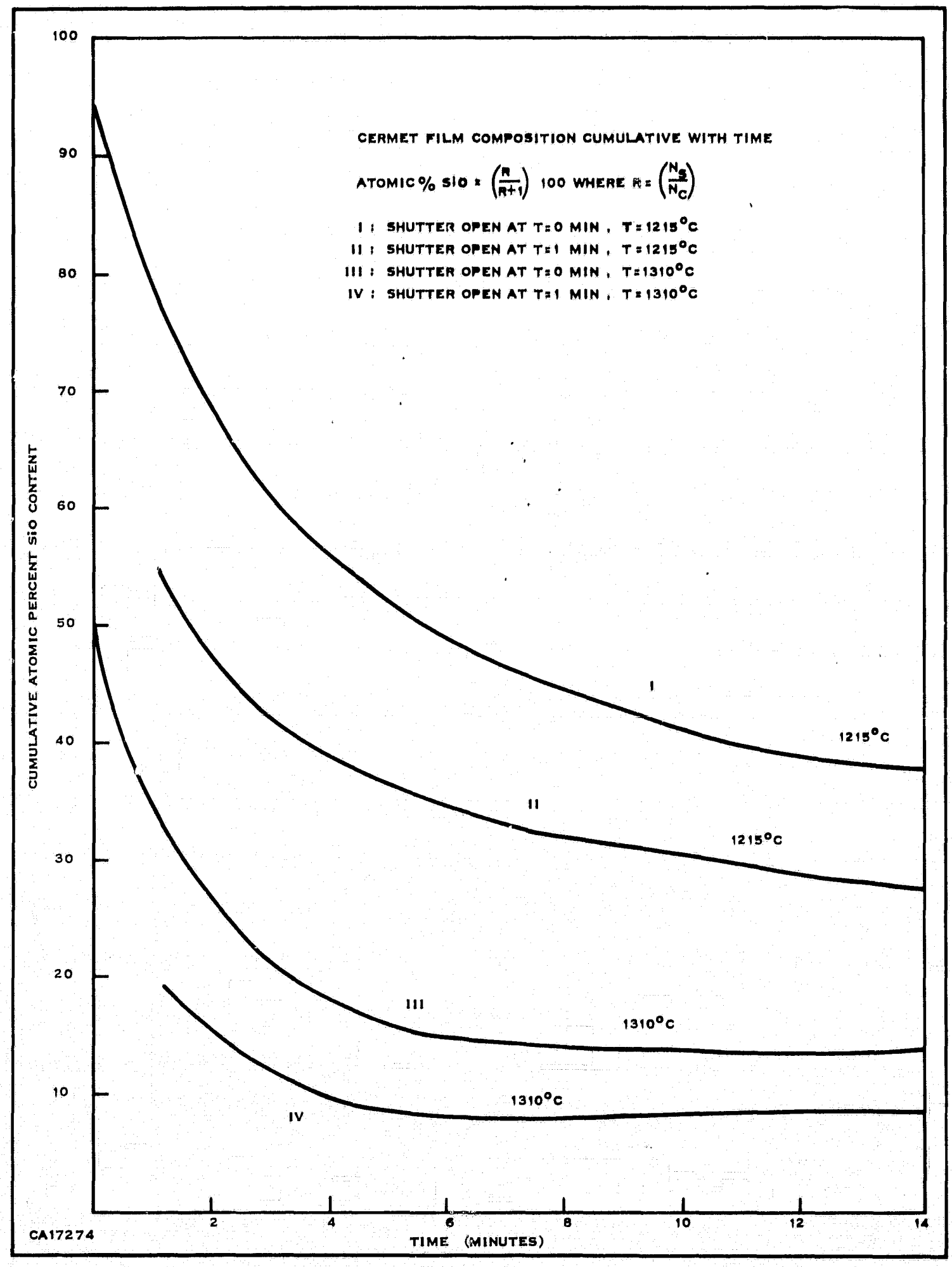


Figure 36. Cermet Film Composition Cumulative with Time

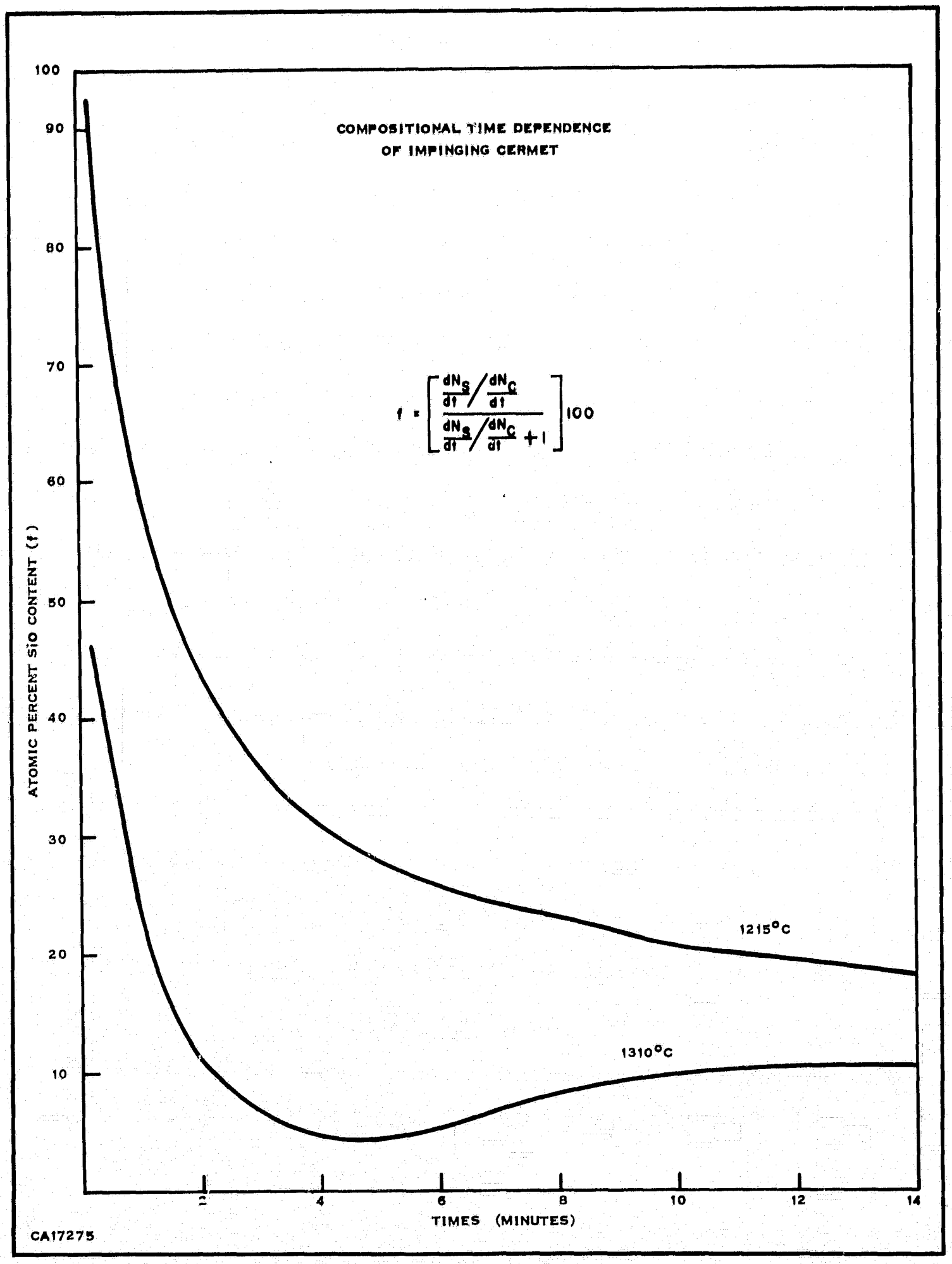


Figure 37. Compositional Time Dependence of Impinging Cermet

C. EXPERIMENTAL: STRUCTURE AND COMPOSITION OF EVAPORATED CERMET FILMS

A series of cermet deposition runs, which will be described in detail later (numbers 11—16), were made with a view to correlating various properties such as film thickness, composition and resistivity. For these purposes, target slices in each run included two chemically polished single crystal germanium wafers. The deposited cermet was then analyzed for chromium and silicon content by means of an electron microprobe analyzer. The data is recorded in Table 11, together with thickness measurements which were obtained by ellipsometry.

Table 11. Electron Microprobe Analysis of Cermet Film

Sample Number	Thickness Å	Refractive Index (n)	K_{cr}	K_{si}	K_{cr}/K_{si}	Max. Error 90% Cont.
11-4	980	2.66-0.6i	0.0698	0.0229	3.04	±0.2
11-7	1050	2.6 -0.6i	0.0703	0.0233	3.02	±0.2
12-4	100	2.1 -2.0i	0.0345	0.00478	7.21	±1.5
12-7	110	2.49-2.0i	0.0402	0.00838	4.92	±1.5
13-4	110	2.66-1.8i	0.0150	0.00428	3.50	±2.0
13-7	100	2.37-1.8i	0.0133	0.00308	4.31	±2.0
14-4	340	2.16-0.2i	0.0608	0.0522	1.16	±0.2
14-7	340	2.14-0.2i	0.0682	0.0591	1.16	±0.2
15-4	570	2.26-0.5i	0.0720	0.0920	0.783	±0.1
15-7	530	2.31-0.4i	0.0615	0.0886	0.695	±0.1
16-4	50	2.39-2.0i	0.0141	0.00053	26.5	±5.0
16-7	50	2.40-2.0i	0.0144	0.00106	13.6	±5.0

The electron microprobe analysis was carried out by monitoring the C_rK_α and S_iK_α X-ray emissions while an exciting electron beam of 25 kV energy was focused to 5-micron diameter spots on the films. Several 100-second counts were taken at each spot. These intensities were compared to the intensities excited from pure chromium and silicon. The ratios of K_{cr}/K_{si} should be quite close to the weight ratio of C_r/S_i. The intensity ratios are defined

$$K_{Cr} = \frac{I^{s}_{Cr} - I^{Bk}_{Cr}}{I^{\circ}_{Cr} - I^{Bk}_{Cr}} \quad , \qquad K_{si} = \frac{I^{S}_{Si} - I^{Bk}_{Si}}{I^{\circ}_{Si} - I^{Bk}_{Si}}$$

where I°_{Cr} is chromium Ka_1 intensity from pure chromium, I^{Bk}_{Cr} is the background, and I^{s}_{Cr} is the $CrKa_1$ intensity from the sample. Similar definitions apply for Si. The error is defined by:

$$E = 2\left[\frac{I^{\circ}_{Cr} - I^{Bk}_{Cr}}{(I^{\circ}_{Cr} + I^{Bk}_{Cr})^2} + \frac{I^{s}_{Cr} + I^{Bk}_{Cr}}{(I^{s}_{Cr} + I^{Bk}_{Cr})^2} + \frac{I^{\circ}_{Si} + I^{Bk}_{Si}}{(I^{\circ}_{Si} + I^{Bk}_{Si})^2} + \frac{I^{s}_{Si} + I^{Bk}_{Si}}{(I^{s}_{Si} + I^{Bk}_{Si})^2}\right]^{1/2}.$$

X-ray diffractometer analysis of the cermet films on germanium wafers contained no evidence of crystallinity (on an X-ray scale) in any of the films examined. It may be concluded from this that the chromium is finely dispersed so as to be effectively amorphous. The SiO cannot be expected to show any pattern, since no crystalline habit is known to exist (46). This was confirmed when a sample of SiO granules (uncrushed) gave no diffraction pattern with X-rays.

Electron micrographs were taken of replications of Cr-SiO cermet films deposited on $Si_3N_4 - SiO_2 - Si$ sandwich wafers. Figure 38 shows a 62,500 X view of a surface after deposition at 200° C substrate temperature before anneal; Figure 39 shows the appearance after a 400° C vacuum anneal for 30 minutes. Considerable decrease in grain size is evident and contradicts the evidence of Glang, Holmwood and Herd (20). No explanation is offered for this apparent behavior, or whether it is in fact characteristic of films evaporated from the mix.

D. EXPERIMENTAL: CERMET RESISTOR DEPOSITION

1. Evaporator System Used To Form the Cermet Resistor

A simple oil diffusion, liquid nitrogen trapped vacuum system was used for the cermet evaporations to be described in this report. With the ionization gauge located outside of the bell jar, the system was capable of pressures of about 2×10^{-7} torr.

Resistor deposition was achieved by downward evaporation of a cermet powder mixture contained in a resistance heated boat arrangement shown in Figure 40. The top and bottom portions are of 0.010-inch thick tungsten and are commercially available as type S-31 from R.D. Mathis and Company. A common problem in boat systems such as this is making a simple versatile electrical connection to the tungsten. It is common practice to use end jaws which hold top and bottom portions together. Unfortunately, the high temperatures encountered frequently result in mechanical "freezing" of these parts, which, coupled with the extreme brittleness of the tungsten, make repeated boat dismantling impractical. Modification of the lower boat by bending

Figure 38. Cermet Film Before Alloy (X62500)

Figure 39. Cermet Film After Alloy, 400 Degrees C Vacuum, 30 Minutes (X62500)

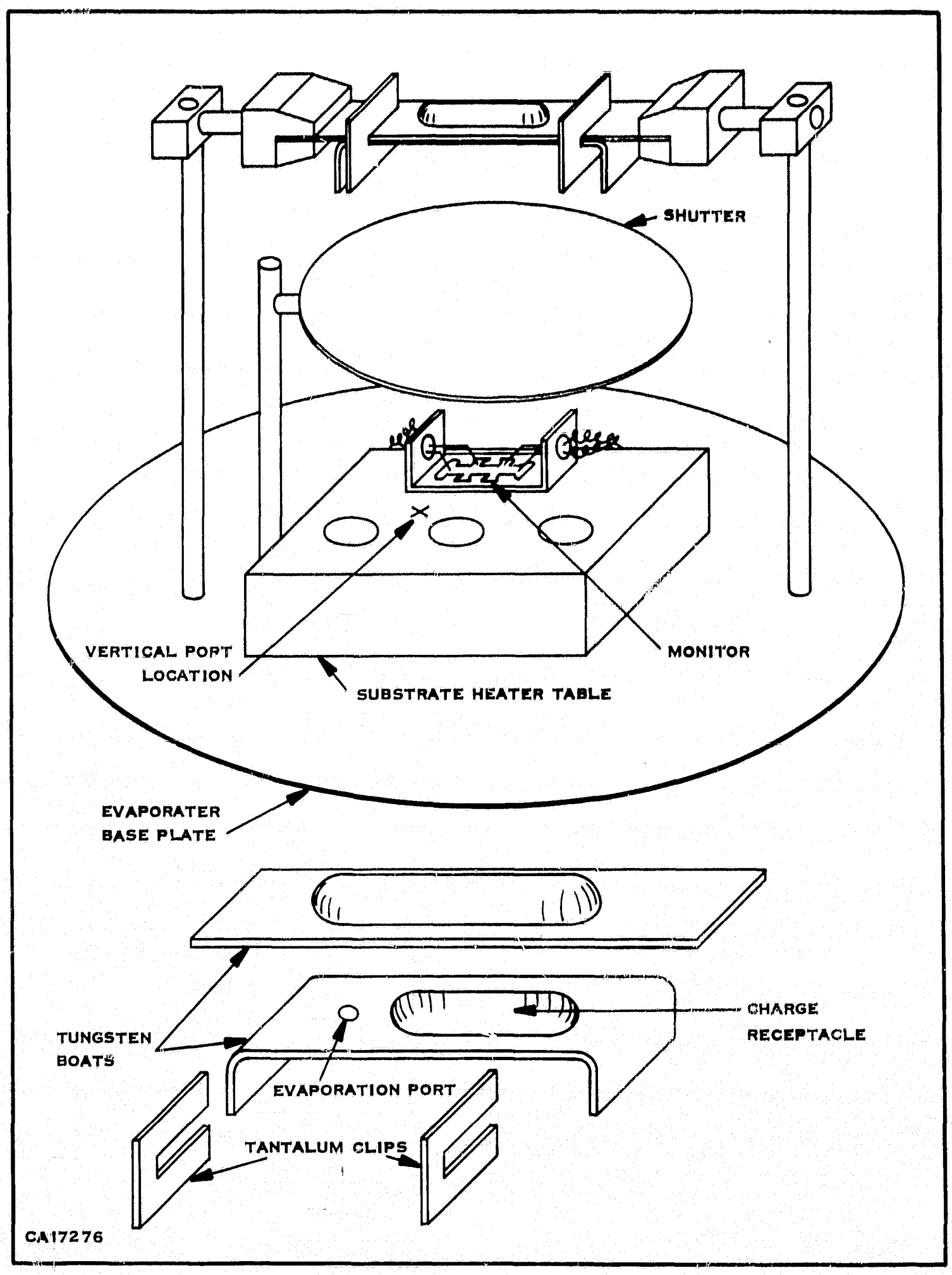


Figure 40. Evaporator Setup for Cr-SiO Cermet Deposition

the ends at right angles and use of tantalum clips to attach to the top section results in a convenient low-cost demountable arrangement, permitting predeposition firing and repeated boat usage, with less outgassing the primary resulting advantage. Resistance heating current flow takes place primarily through the top heater with the resulting disadvantage that the lower section is cooler and the effective temperature of the source charge is less well defined than if both sections were resistively heated.

Source to substrate distance was approximately 6 inches, with target slices placed face upward on a portable insulated stainless steel table heated from below by quartz incandescent tubes. Temperatures of 500°C were attainable, monitored by a thermocouple. An externally operated manual shutter was located between source and target. Source filament and jaw clamps were partially enclosed in a removable radiation shield.

2. Charge Preparation

The cermet charge powder is a mixture of 80% chromium and 20% silicon monoxide by weight. On an atomic basis this is 77.1 atomic percent chromium and 22.9 atomic percent silicon monoxide. The chromium is obtained in 300 mesh powder form containing copper as the dominant impurity, 1–10 ppm. The silicon monoxide is Kemet Select Grade #10 mesh vacuum baked, and was mechanically pulverized to a fine powder form and thoroughly mixed with the chromium in the above-mentioned ratio.

3. Conditions During Deposition

On general principles alone, it was felt desirable from the beginning to maintain as good a vacuum as possible during deposition. Subsequent experience has indicated that vacuum degradation can exacerbate resistance control problems such as post-deposition air aging, or changes arising during pattern definition or assembly. The factors affecting vacuum degradation will be discussed in order of their occurrence during operation, assuming that the pump system itself is in satisfactory operational condition.

In the course of evaporating Cr-SiO cermets repeatedly in the same system, the baseplate, fixtures and bell jar become quite heavily coated with cermet deposits. These are predominantly SiO because in evaporation a significant fraction of the initial charge remains behind in the form of chromium. These multiple layers of SiO will ordinarily absorb gases, and particularly water when the bell jar is raised. Reduction in pumping speed has been directly correlated with duration of exposure to room air, but can be recovered by prolonged pumping and outgassing of the system. In practice, it is advisable to minimize this sort of exposure of the internal bell jar system.

A thorough outgassing of cermet charge and target slices is also required prior to deposition. The deposition sequences in Figures 49 to 54 show the use of 100 to 200 amperes in this operation, though the most significant release of water and absorbed gasses is felt to take place at 100 amperes in five minutes or less. Target slice outgassing is achieved by heating to 450° C for 30 minutes prior to deposition. Generally, the pressure transient is smaller than when the charge is heated.

The most severe outgassing problem occurs during deposition, when an excessive temperature rise of the fixtures internal to the bell jar can occur, due to the intense radiation from the filament. In a prolonged deposition the bell jar and baseplate will also experience temperature rise. Predeposition outgassing by prolonged heating and pumping and minimal air exposure help alleviate this problem. In the event of a need for a prolonged deposition, it has been found best to interrupt the cycle and allow for cooling and vacuum improvement, on a repeated basis if necessary.

Most depositions were carried out with filament current set at 275 amperes. It should be remembered that most of this current travels through the upper half of the filament arrangement, resulting in a temperature differential between top and bottom. These temperatures were evaluated with an optical pyrometer (uncorrected) at two current levels.

250 amperes	Top 1340°C
	Bottom 935°C
	Mean 1140°C
275 amperes	Top 1385°C
	Bottom 1037°C
	Mean 1211°C

The temperature differential between top and bottom is quite large and, consequently, reduces the accuracy of estimates of charge temperature. Furthermore, experimental variations from the above estimates could arise from variations in thermal/physical contact between upper and lower filament members as well as size of cermet charge mass.

Sheet resistance of the deposited film was monitored by a four-terminal method to eliminate possible contact resistance errors. The choice of monitor materials and temperature was governed by a desire to duplicate as closely as possible the conditions of deposition on the target slices. The binary counter circuit specified in this contract called for silicon substrate material with planar oxide coated with

silicon intride. Monitors were fabricated by first cavitroning standard Hall bar samples, Figure 41, from chemically polished silicon. Edge roughness was subsequently removed by light chemical etching. This was followed by oxidation to 5000Å and then Si_3N_4 deposition to 1000Å. Evaporated aluminum contacts were then applied as shown. For deposition, the monitor was placed in a spring contact fixture, Figure 40, resting on the substrate heater table. This demountable arrangement was very convenient and assured monitor duplication of target slice deposition conditions.

The normal cermet deposition cycle used consists of the following basic procedures, after insertion of slices, monitor and charge.

1) Pump down to $2\text{-}4 \times 10^{-7}$ torr.
2) Outgas target slices at 450° C. Lower temperature to 200° C.
3) Outgas cermet powder charge at 100–200 amperes with shutter closed. Allow retrieval from increased pressure if necessary.
4) Commence deposition at 250–275 amperes. Shutter action optional, depending on desired film compositions and final sheet resistance.
5) Anneal slices at 400°C for 5–10 minutes. Recent literature (20) indicates the desirability for a minimum 60-minute anneal at least at 400° C, preferably at 500° C.

The validity of monitor sheet resistance measurements naturally raises the question of deposition uniformity. The substrate table could conveniently accommodate three slices in addition to the monitor. To evaluate thickness uniformity of deposition, six microscope slides were added to an early experimental run in close location to one slice and monitor. The interferometrically determined thickness values taken approximately in the center of each slice were, in angstrom units: 417, 474, 590, 500, 500, 553. The two slices on either side of the center slice measured 590Å and 500Å. Absolute accuracy was ±100A, but data is given to three digits on the basis of precision. These variations were considered acceptable in the initial phases of this study.

4. Photolithographic and Contact Process

The technique used to define cermet resistor geometry was the reverse aluminum method, which is particularly compatible with some integrated circuit processes. Other methods, such as photolithographic etching with HF-HCL mixtures have been used (29), but problems can arise from the HF attack of the exposed SiO_2 at window edges when a top coating of Si_3N_4 is used. Due to temperature considerations, the cermet deposition is usually the final process step in the fabrication of a composite

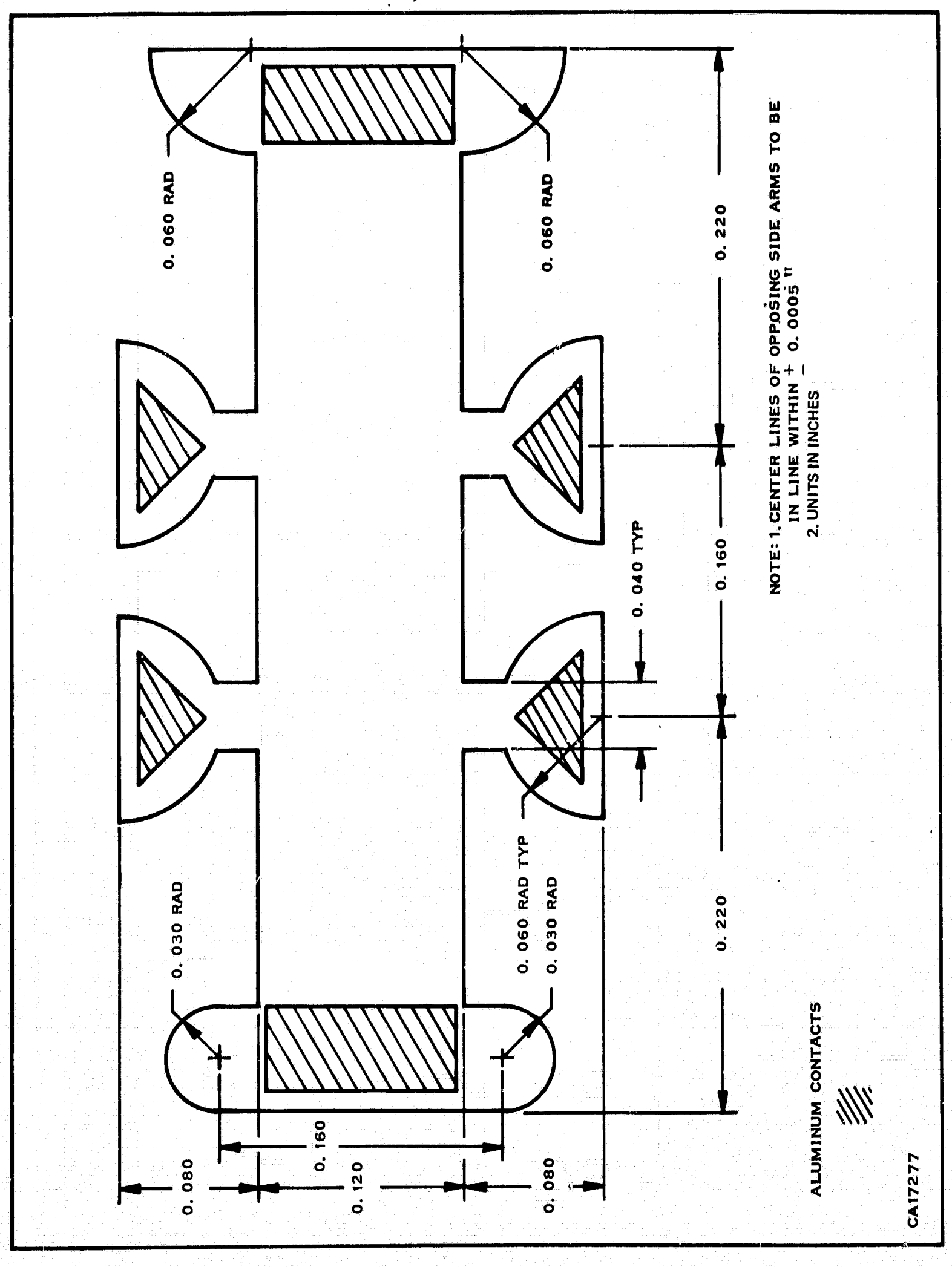


Figure 41. Sample Shape for Bridge-Type Hall Bars

integrated circuit. If the silicon diffusions form sufficiently degenerate regions, aluminum can make adequate contact during the annealing step; otherwise, a defined alloy metallization step is needed prior to cermet deposition.

In either event, the reverse aluminum deposition method consists of the following steps:

1) Aluminum evaporation over entire slice held at room temperature.
2) Reverse photolithographic definition of the resistor pattern in the aluminum. That is, the aluminum is removed where the cermet is to be located.
3) Cermet deposition and anneal.
4) Resistor definition as follows: immerse slice in 0.1N KON solution in half full beaker at room temperature. Place beaker in ultrasonic water bath until the resistor is defined. The latter step is necessary to help penetration of KOH to the underlying aluminum, whereupon dissolution takes place followed by dislodgement of the cermet overlayer. Typical examples of partially etched and completed resistors are shown in Figures 42 and 43. Etch removal time is of the order of 20—30 minutes. This is followed by a five-minute rinse in deionized water.
5) Aluminum evaporation over entire slice.
6) Conventional photolithographic definition of aluminum contacts and interconnects.
7) Anneal-alloy cycle, 400°C, 30 minutes in dry nitrogen. This is a dual-purpose step designed to lower contact resistance and simultaneously anneal the cermet film. Annealing behavior encountered in this contract effort has shown considerable variation. On the basis of experience and observations in the literature it can be said that this is due in large part to compositional variations in the deposited film which can be due to a variety of causes. This forms a critical part of the technology and will be discussed fully in this report.

Three types of resistor patterns were used in this study. Initially, the patterns depicted in Figures 44 and 45 were used in order to evaluate resolution capability and effects of aspect ratio and contact resistance. The binary counter resistor pattern is shown as part of the final circuit in Figure 8, where it can be seen that the reverse aluminum technique has a demonstrated capability of defining cermet stripes 0.4 mil in width with 0.4 mil separation.

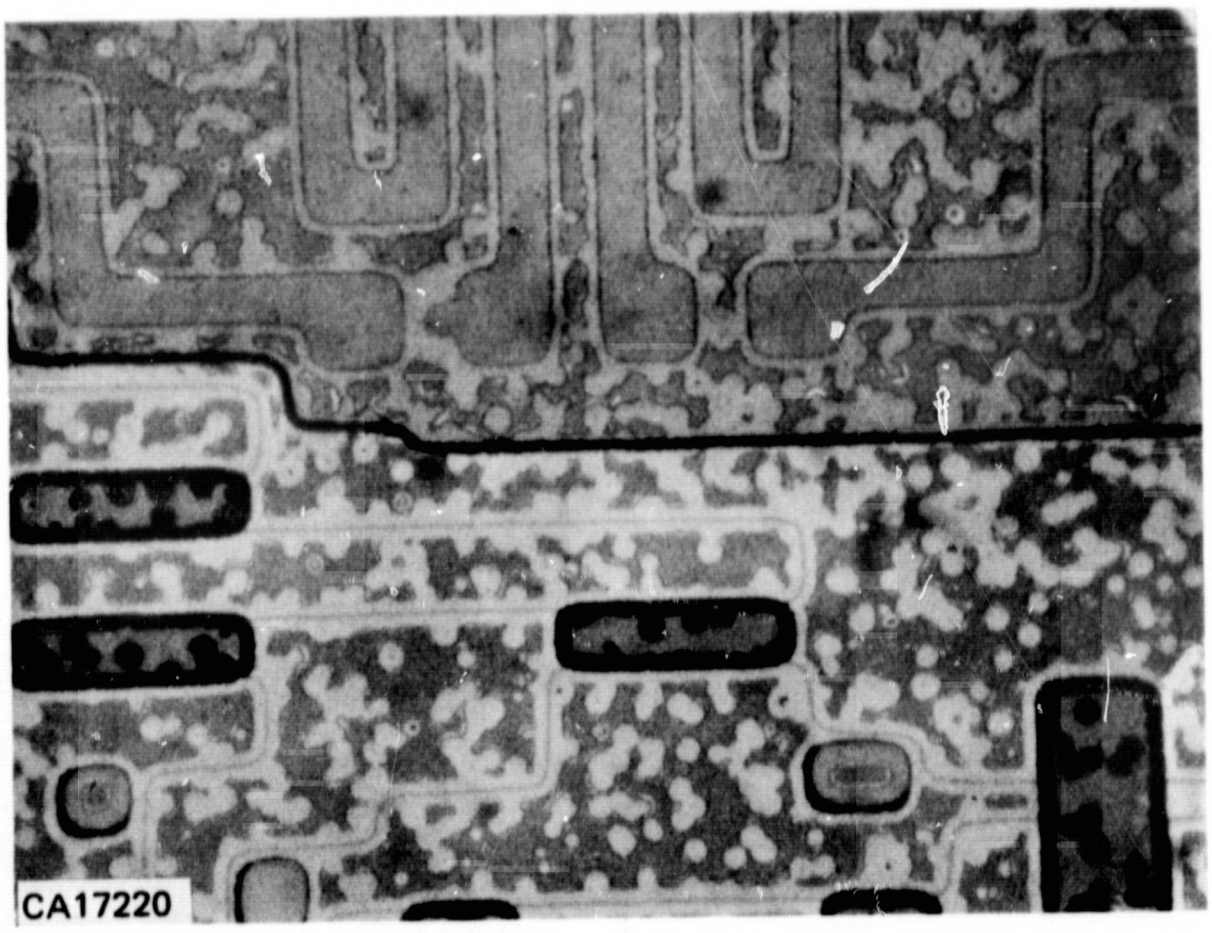


Figure 42. Partially Etch-Removed Cermet

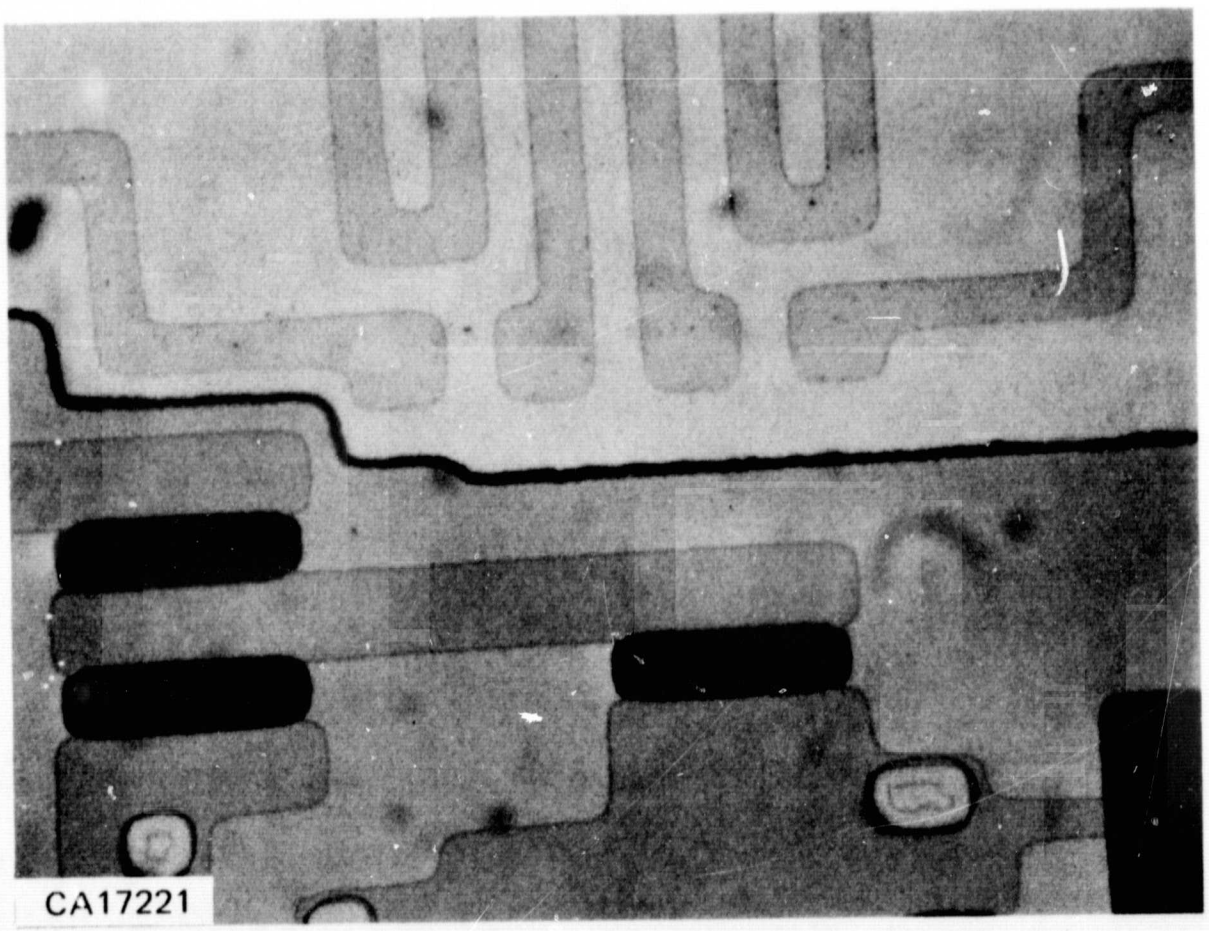


Figure 43. Completely Defined Cermet

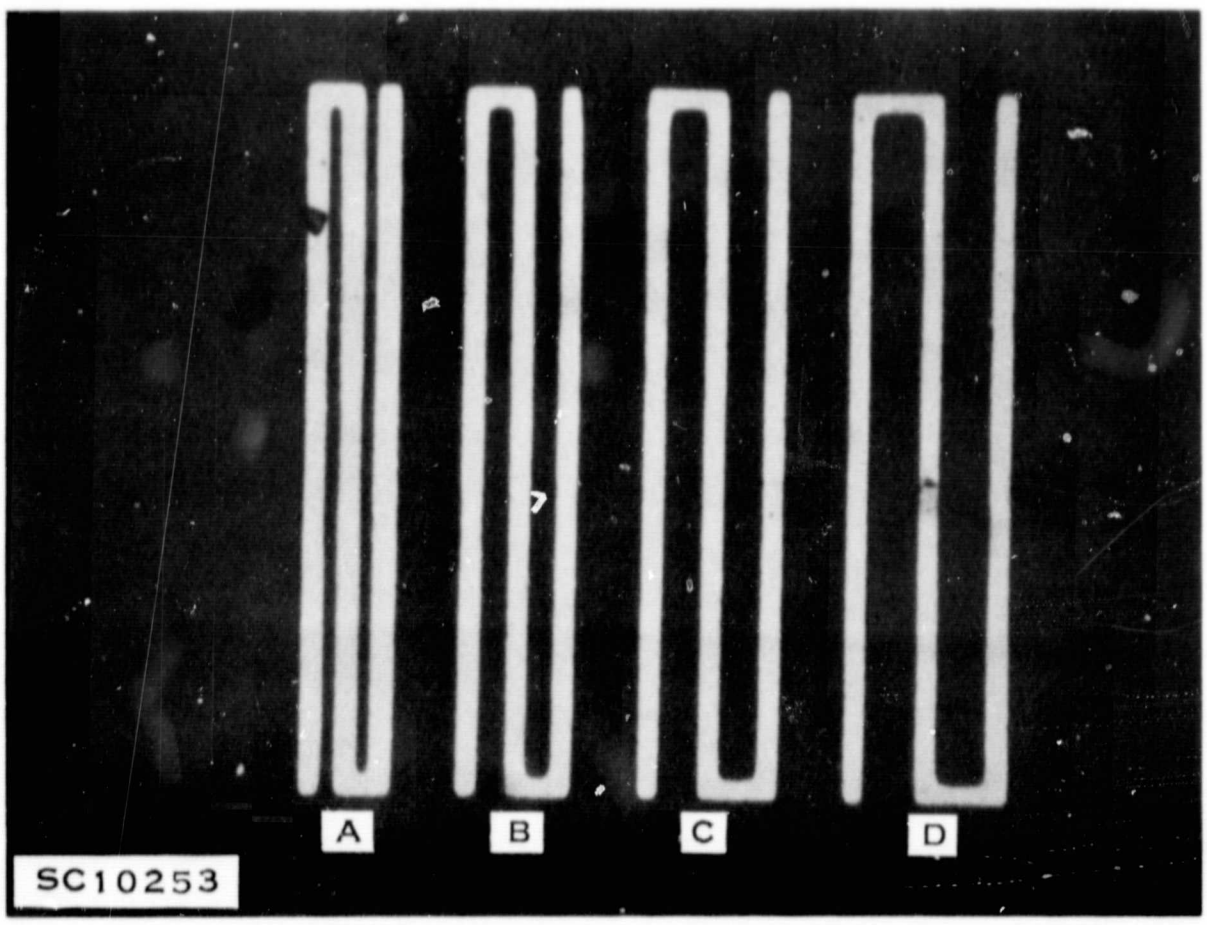


Figure 44. Example of Resistor Resolution Capability. Resistor Widths Are 0.2 Mil. Spacing Between Resistors A, B, C, and D Are 0.1, 0.2, 0.3, and 0.4 Mil, Respectively

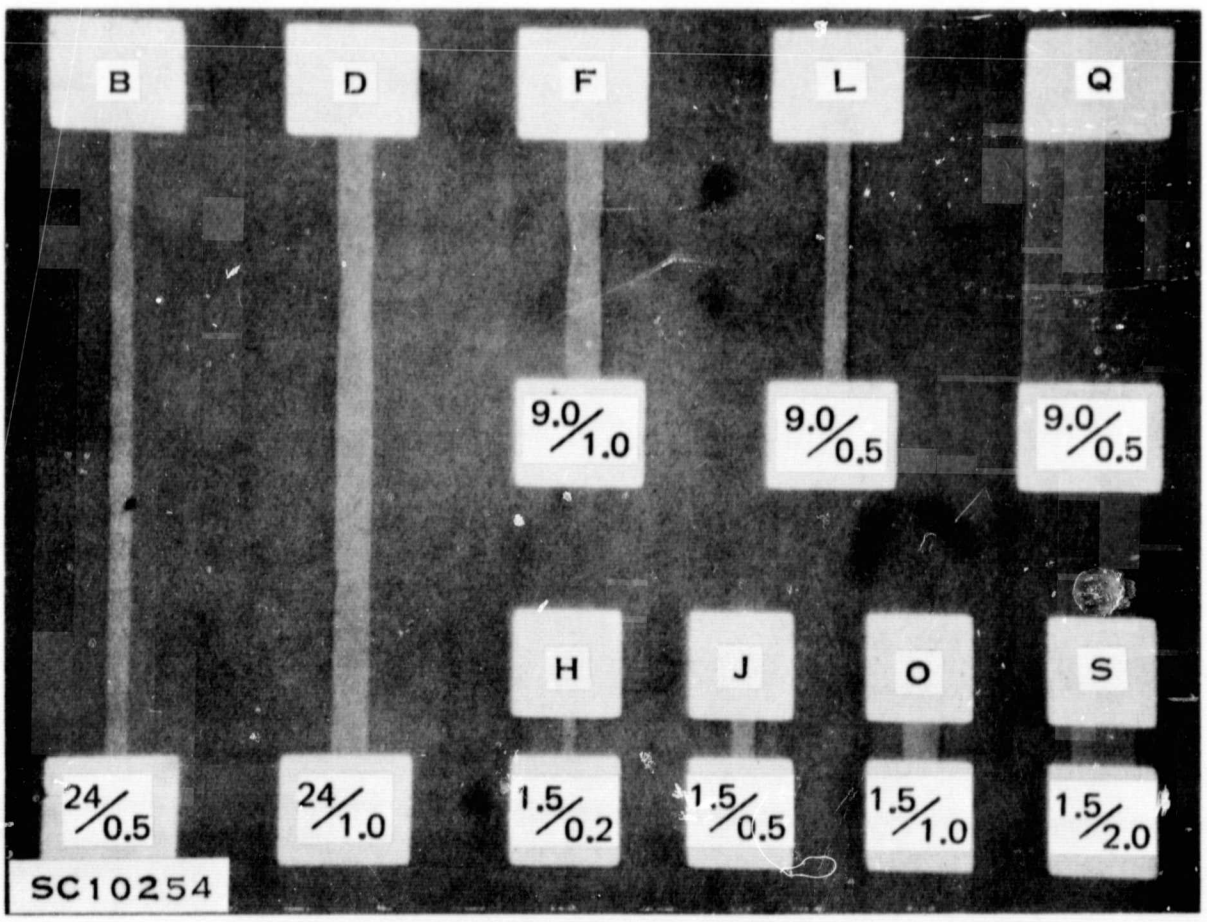


Figure 45. Test Pattern for Measurements of Resistance and TCR Values. Configuration Is Designated by Letters in the Uppermost Contact Lands. The Length to Width Ratios (in mils) Are Shown in the Lower Lands

NOTE:

CONFIGURATION B, RUN NO. 5
NOMINAL RESISTANCE = 240 KΩ

$$\text{CALCULATED TCR} = \frac{\Delta R}{R \Delta T}$$

$TCR_I = 1.44 \times 10^{-4}$
$TCR_C = 1.55 \times 10^{-4}$
$TCR_A = 1.36 \times 10^{-4}$
$TCR_J = 1.40 \times 10^{-4}$

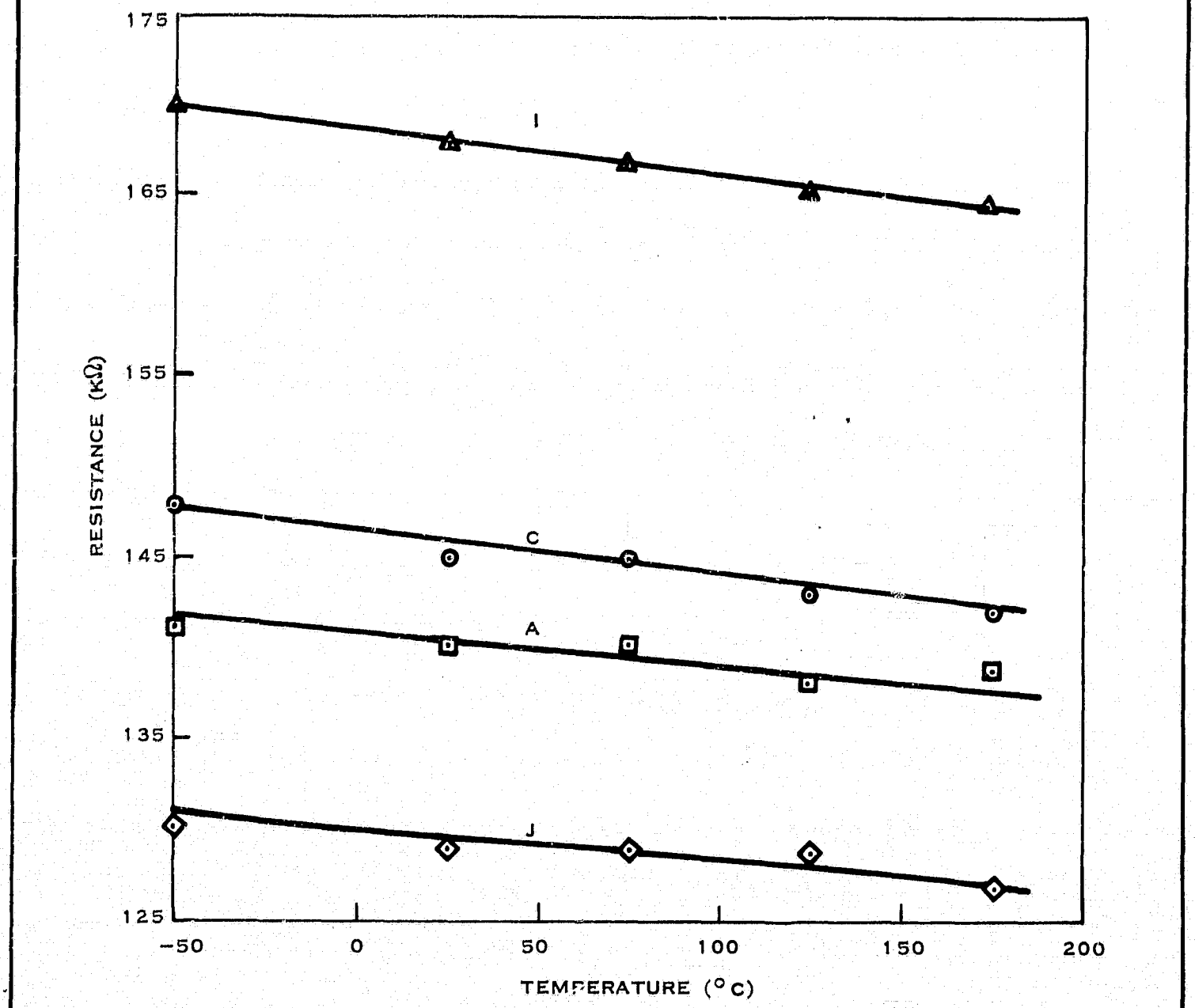


Figure 46. Variation of Cermet Resistance with Temperature

5. Assembly

In the developmental techniques used in this study, the resistors and MNOS transistors were probe evaluated prior to assembly. Individual chips were prepared by lapping the back of the wafer, evaporating phosphorus-doped gold on the lapped face, scribing, and breaking. The chips were alloyed to TO-5 8-pin headers at 425°C for a period of 1—1-1/2 minutes (approximately) in a jet atmosphere of forming gas. One-mil (0.001 inch) gold wires were bonded to the aluminum contact lands. Hermetic cap welding was performed in dry nitrogen ambient.

E. EXPERIMENTAL: TEMPERATURE COEFFICIENT OF RESISTANCE OF CERMET RESISTORS

The temperature dependance of resistance in cermet thin-films has been investigated widely and was discussed in Section III-A of this report. It is apparently very dependent on composition and thermal history. The compositional nonuniformity that occurs in the films studied under this contract make it extremely difficult to perform any useful correlations with literature values.

Three sets of resistance-temperature curves that have been obtained in the course of this work are shown in Figures 46, 47 and 48. It should be pointed out that Run #19, Figure 47, was the one from which units were selected for delivery under the terms of this contract. TCR here was approximately zero ppm/°C at a sheet resistance of about 4400 ohms/square. The temperature coefficients of resistance, as measured, range from approximately 0 to −170 ppm/°C and appear to be more or less constant over a temperature range −50° C to 150° C for each resistor examined.

F. EXPERIMENTAL: RELATION OF DEPOSITION CONDITIONS TO FILM PROPERTIES FOR INDIVIDUAL RUNS

The resistor deposition run numbers are in chronological sequence. Most of the early depositions were exploratory, in some instances carried out simply to evaluate the mechanics of the deposition process such as outgassing, temperature measurement, etc., where resistors were not deposited. The runs where no useful depositions were made are not reported.

Run 11. Figure 49

A cleaned, new boat system was charged with a relatively large amount of Cr-SiO mixture, 386 mg. Runs 11, 12 and 13 were to be deposited in sequence using the same charge to observe the effects of selective compositional depletion of the same mixture. In Run No. 11 the rate of resistor buildup was very rapid, most likely due in part to the relatively good vacuum ($<10^{-5}$ torr.) during the 275A deposition and also to the large charge mass used.

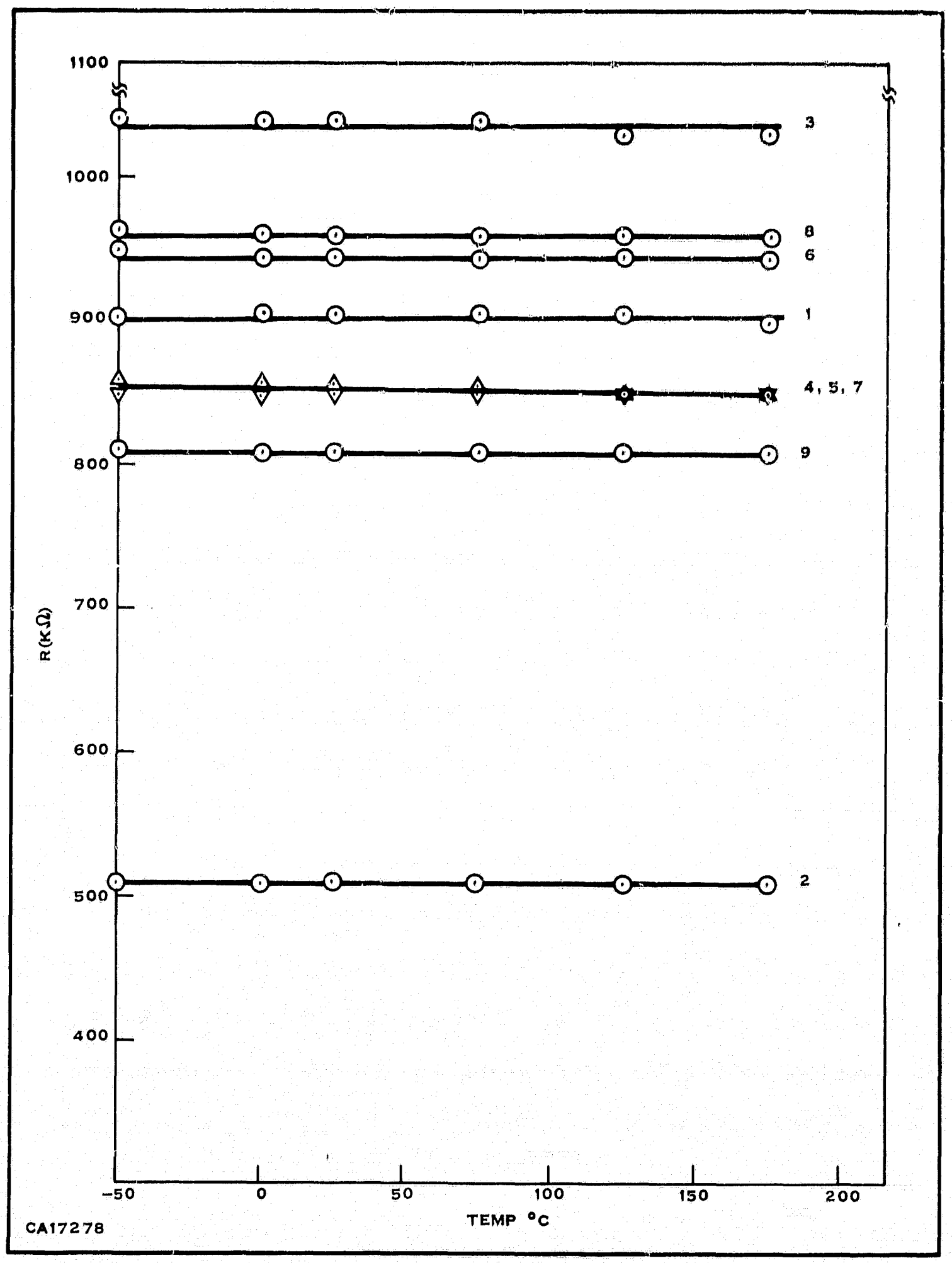


Figure 47. Variation of Cermet Resistance with Temperature—Run Number 19

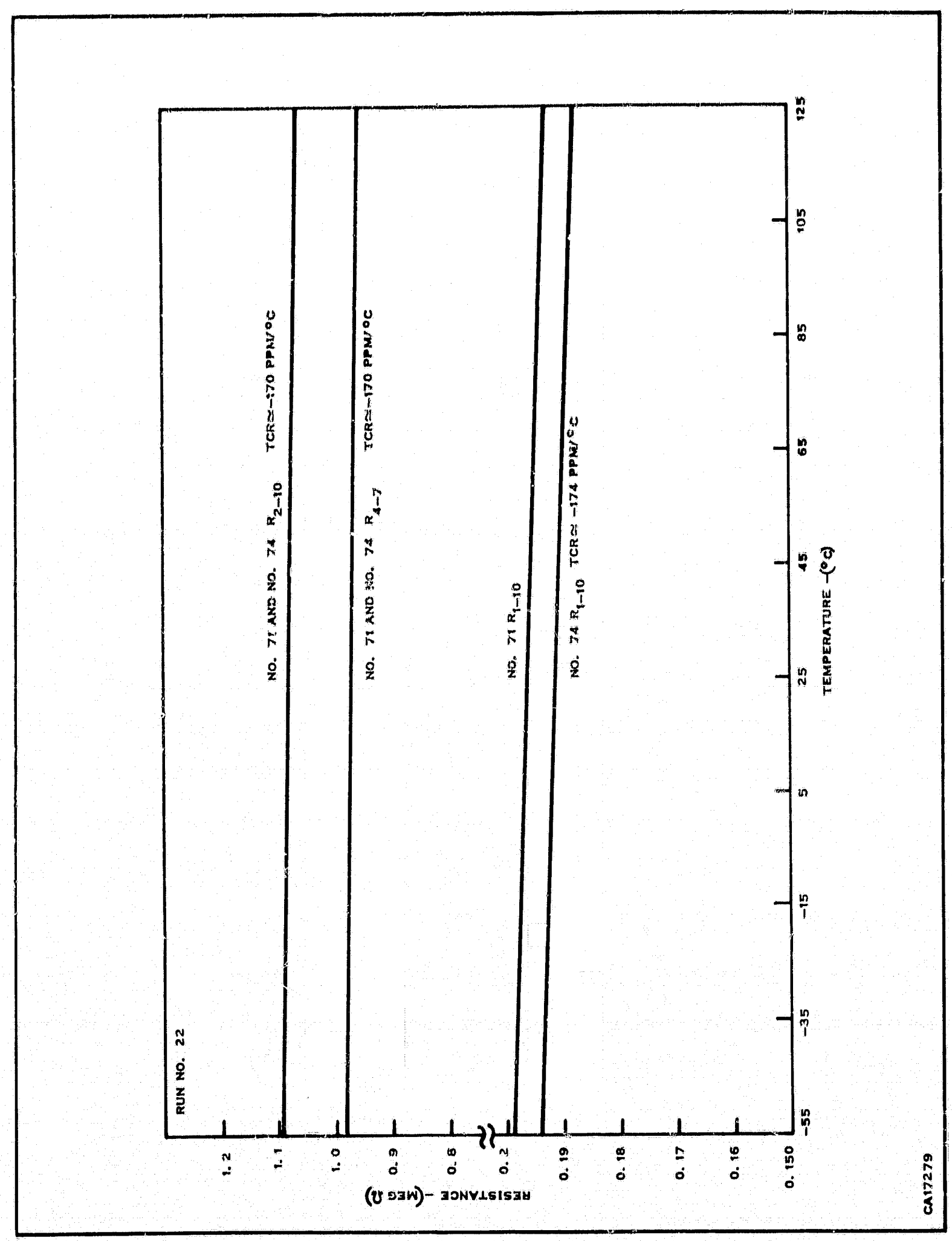


Figure 48. Variation of Cermet Resistance with Temperature— Run Number 22

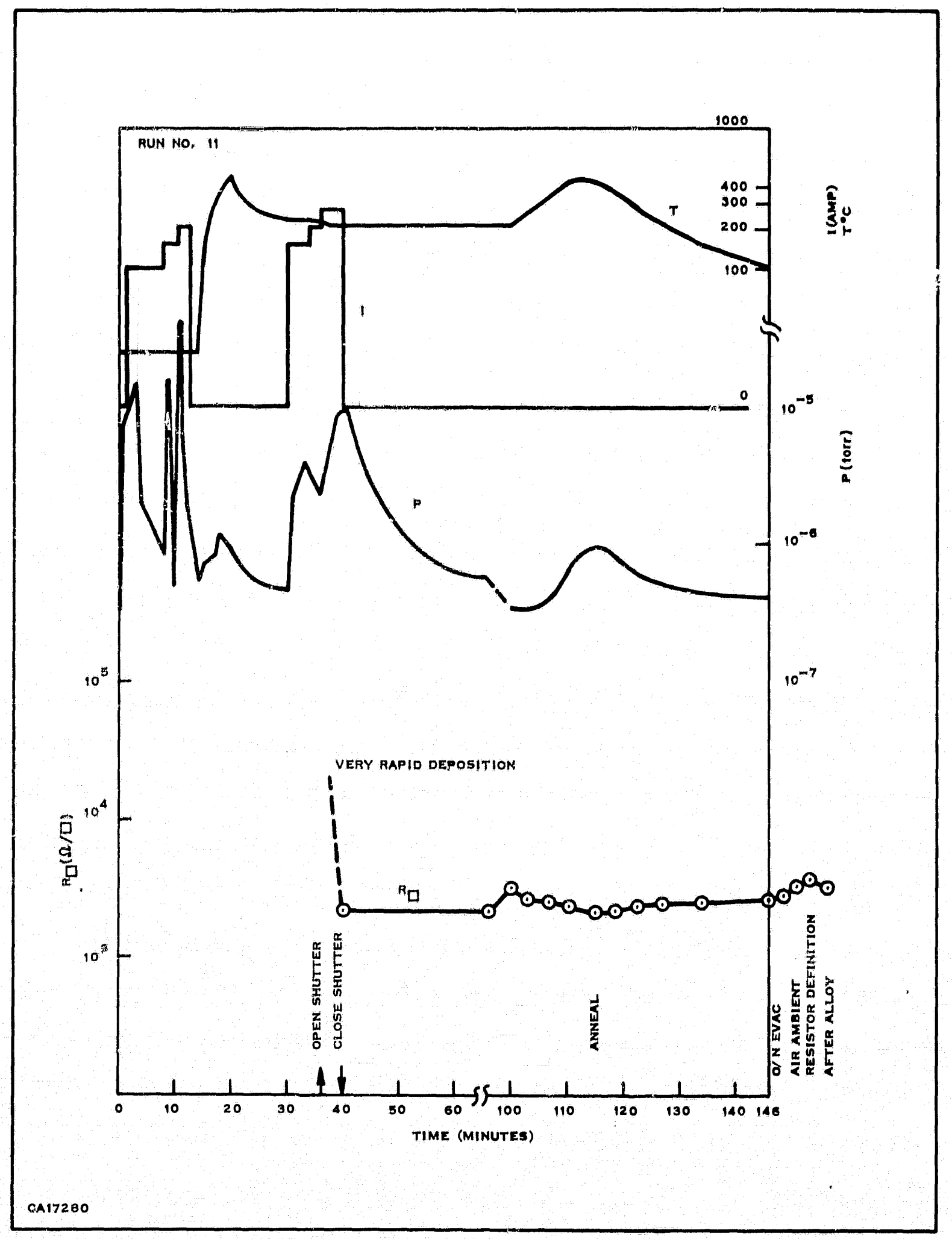


Figure 48. Deposition Conditions — Run Number 11

Resistance increase due to air age was approximately 50%; however, no drastic changes were observed for the resistor definition or alloy operations. Electron microprobe analysis of films deposited on neighboring germanium slices indicates an SiO content at the 38 atomic percent level (higher than the 23% value for the mixture). This suggests that the SiO has been sublimed off more rapidly than the Cr, as is to be expected from its higher vapor pressure. With a large SiO content a thickness of 980–1050Å was required to achieve a sheet resistance of 2220 ohms/square under deposition conditions. Inspection of Figure 35 shows that a 38 atomic % composition is reached in a three-minute deposition cycle at 1215°C, preceded by a one-minute deposition with shutter closed. Since the preheat operation, 4-1/2 minute at 200 amperes, is equivalent to considerably less than one minute at 275 amperes (see discussion of Run #13), we must conclude that effective filament temperature lies somewhere between 1215°C and 1310°C.

Run 12. Figure 50

In this deposition the depleted charge from Run No. 11 was reused. To avoid excessive deterioration of vacuum due to outgassing, the deposition cycle was interrupted to allow for cool down and vacuum improvement. Electron microprobe data shows a lowered SiO content of about 24 atomic %. Higher chromium content is to be expected in view of the preferential loss of SiO in Run No. 11. Total deposition time at 275 amperes was six minutes. Examination of Figure 36 from four to ten minutes shows that the deposit composition of the 1215°C curve ranges from 30 to 20 atomic % SiO, whose mean is close to the measured value of 24%.

Run 13. Figure 51

As in Run No. 12, the same depleted charge was used as deposition source. An interrupted deposition sequence was again dictated by outgassing. In spite of this precaution, pressure was about 10^{-5} torr. during deposition to a sheet resistance of 3300 ohms/square. On cooling resistance increased, and exposure to air resulted in further air age. Consequently, it was decided to perform a second deposition to further lower sheet resistance. Considerable difficulty was encountered in achieving a resistance decrease. Outgassing was quite noticeable; in fact, during most of the 275 ampere intervals the pressure was between $1 - 2 \times 10^{-5}$ torr. This strongly suggests the chromium fraction was being oxidized rather than sublimed (chromium is noted for its gettering properties); this resulted in a SiO rich deposit. A similar phenomenon was observed in Run No. 8, where some resistance decrease was observed after an extended deposition period. Assuming full oxidation of the chromium, we are in a

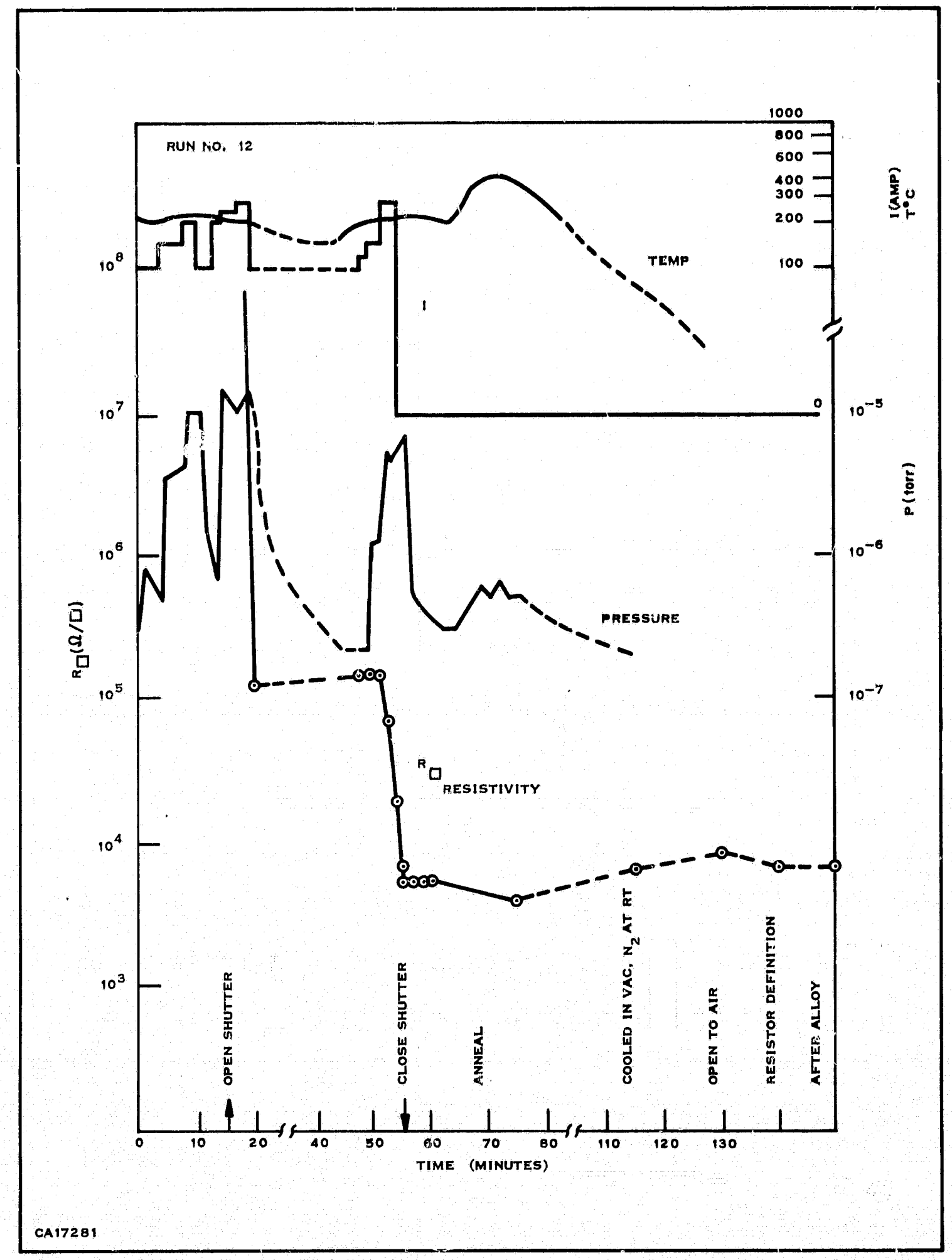


Figure 50. Deposition Conditions-Run Number 12

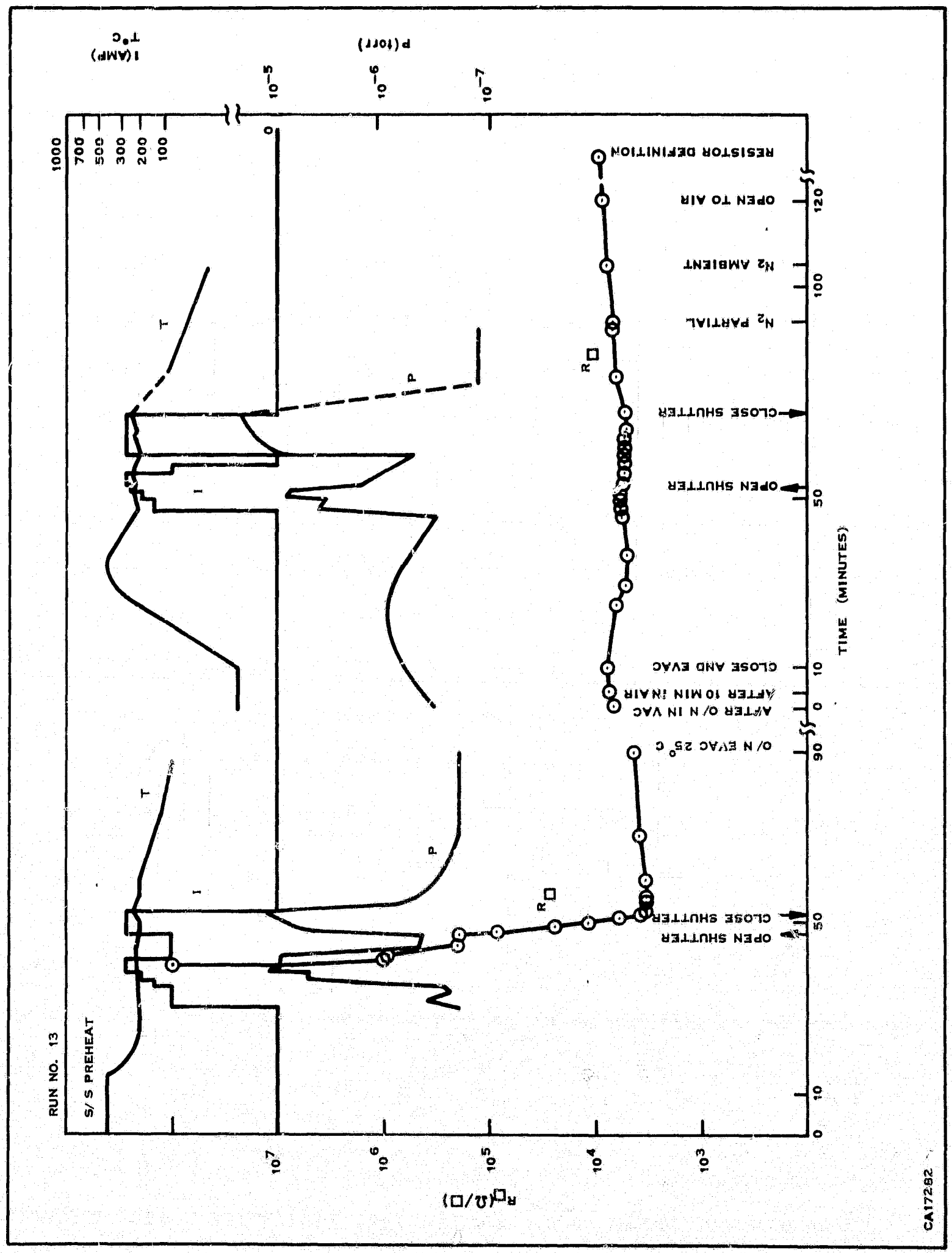


Figure 51. Deposition Conditions —Run Number 13

position to estimate the average SiO content of the deposit, and compare with electron microprobe data. By the start of Run No. 13, the sample heater had been cumulatively subjected to 10 minutes at 275 Amps, plus 3 minutes at 250 Amp, plus 8 minutes at 200 Amps as well as some heating at 150 and 100 Amps which may be effectively discounted from consideration of material loss. It has been observed that 250 Amp heater operation reduces average temperature by about 100°C below that at 275 Amp. The reduction in SiO and Cr vapour pressures is, very approximately, a factor of ten every 100°C in this temperature range. Consequently the deposition rate could be expected to decrease somewhat in proportion to the vapour pressure. Thus 3 minute at 250 Amp is roughly equivalent to 0.3 minutes at 275 Amp. At 200 Amps the heater system is sufficiently cool to be neglected as far as material loss over reasonable times is concerned.

Thus we may consider the first deposition of Run No. 13 as having a starting point t = 13 min. at 1215°C. Figure (37). Although the Time of Flight Mass Spectrometer data cuts off at t = 14 minutes we may estimate the 5 minute deposit as averaging about 17% SiO. For the second 13 minute deposition let us assume zero chromium content and a deposition rate of SiO comparable to that in the previous deposition. This results in an increased overall average SiO content of 42 at %. Electron microprobe data indicates about 33 atomic % SiO suggesting again that the effective filament temperature is higher than the value of 1215°C assumed in this calculation.

Estimations of relative thicknesses to be expected from Runs 11, 12 and 13 are dependent on assumptions concerning actual filament temperature. From a knowledge of the mean atom ratios of SiO to Cr in the film, and assuming bulk values for film density, and that relative contributions to film thickness of the two constituents are additive (16), we obtain

$$\frac{t_s}{t_c} = \frac{N_s}{N_c} \frac{\rho_c}{\rho_s} \frac{M_s}{M_c}$$

Since the number of atoms (molecules) of species x deposited on area A cm^{+2} to a thickness t cm and density ρ is given by

$$N_x = \frac{GA\rho t}{M}$$

where

G = Avogadro's number

M = molecular (atmoic) weight of species x.

From the Time of Flight Data Figures (34, 35) values of $N_s/N_c = R$ may be obtained for the SiO:Cr atomic ratio being deposited. Using the above invoked assumption of additivity of film thickness,

$$t = t_s + t_c$$

which then allows us to express thickness in terms of t_s which is proportional to the value of cumulative N_s in Figures (34 and 35) which is expressed in arbitrary units.

$$t = t_s \left(1 + \frac{t_c}{t_s}\right)$$

$$= t_s \left[1 + \frac{N_c}{N_s} \frac{\rho_s}{\rho_c} \frac{M_c}{M_s}\right]$$

$$= t_s \left[1 + .35 \frac{N_c}{N_s}\right]$$

where

density of SiO, $\rho_s = 2.2$ approximately

density of Cr, $\rho_c = 7.2$

atomic wt. Cr, $M_c = 52.01$

mol. wt. SiO, $M_s = 44.09$

From Figure (34), the N_s curve gives the cumulative atomic deposition for an effective filament temperature of 1215°C. The contribution to Run No. 11 is seen to be approximately 820 units in the time interval t = 0 to t = 4 minutes, at which time $N_s/N_c = 1.27$

$$t = t_s \left(1 + \frac{0.36}{1.27}\right) = 1.28\ t_s$$

that is, the total film thickness is about 25% greater than the SiO contribution. For Run No. 12, the contribution to N_s in the 4 to 10 minute interval is seen to be 1120 — 820 = 300 arbitrary units. From Figure (33) $\frac{dNs/dt}{dN_{A/dt}}$ is seen to vary from 0.54 to 0.27 in this interval, averaging about 0.4, from which we obtain $t = 1.8\ t_s$. Thus the above calculation predicts a film thickness ratio for Runs 11 and 12 to be

$$\frac{t_{11}}{t_{12}} = \frac{820 \times 1.28}{300 \times 1.8} = \frac{1050}{540} = 1.9$$

whereas Electron Microprobe data yields an average ratio of 1015/105 = 9.7 about five times greater. This discrepancy is not as large as it appears if one considers

the changes in SiO-Cr ratios that may occur due to relatively small changes in effective filament temperature. The above rough calculation is inserted to illustrate that the deposited film characteristics such as composition and thickness are reasonably well understood in their dependence on deposition conditions such as temperature and pressure, which are evidently quite critical.

Run 14. Fig. (52)

The deposition time at 275 Amp was 10 minutes. A fresh boat (prefired) and charge (123 mg) were used. At an effective temperature of 1215°C, Figure (36) indicates an average film SiO concentration of 40 atomic % at t = 10 minutes whereas electron microprobe analysis indicates 61.5 at %. The higher pressures encountered ($1 - 1.2 \times 10^{-5}$ torr) towards the end of the rather prolonged deposition are probably responsible for partial Cr oxidation and preferential deposition of SiO. The purpose of this run was to deposit to a target value of 1000 ohms per square and hopefully utilize the air age effect to trim to a target value of 5000 ohms per square by deliberate post-deposition oxidation. No change in resistance was observed in anneal. The oxidation was performed at 300°C in air ambient of 0.5 to 1.0 torr pressure. After heating for 20 minutes resistance was found to increase only 30%. Surprisingly considerably higher sheet resistance values were noted for the defined resistor patterns.

In estimating the thickness of the deposited film, we need to allow for the mass of charge used. Assuming proportionately between deposition rate and mass, rather than surface area which would be much more difficult to estimate, we obtain,

using $\frac{N_s}{N_c} = 0.7$ for t = 10 minutes and inserting

$$t = 1.50\ t_s$$

and designating film thicknesses for Runs 11 and 14 by t_{11} and t_{14}, and charge masses by m_{11} and m_{14} respectively,

$$\frac{t_{14}}{t_{11}} \equiv \frac{1.50\ t_{s\,14}\ m_{14}}{1.28\ t_{s\,11}\ m_{11}} = \frac{1.50\ N_{s\,14}\ m_{14}}{1.28\ N_{s\,11}\ m_{11}}$$

where

N_{s14} = 1180 (value of N_s at 10 min. 1215°C Figure 34)

N_{s11} = 820 (value of N_s at 4 min, 1215°C)

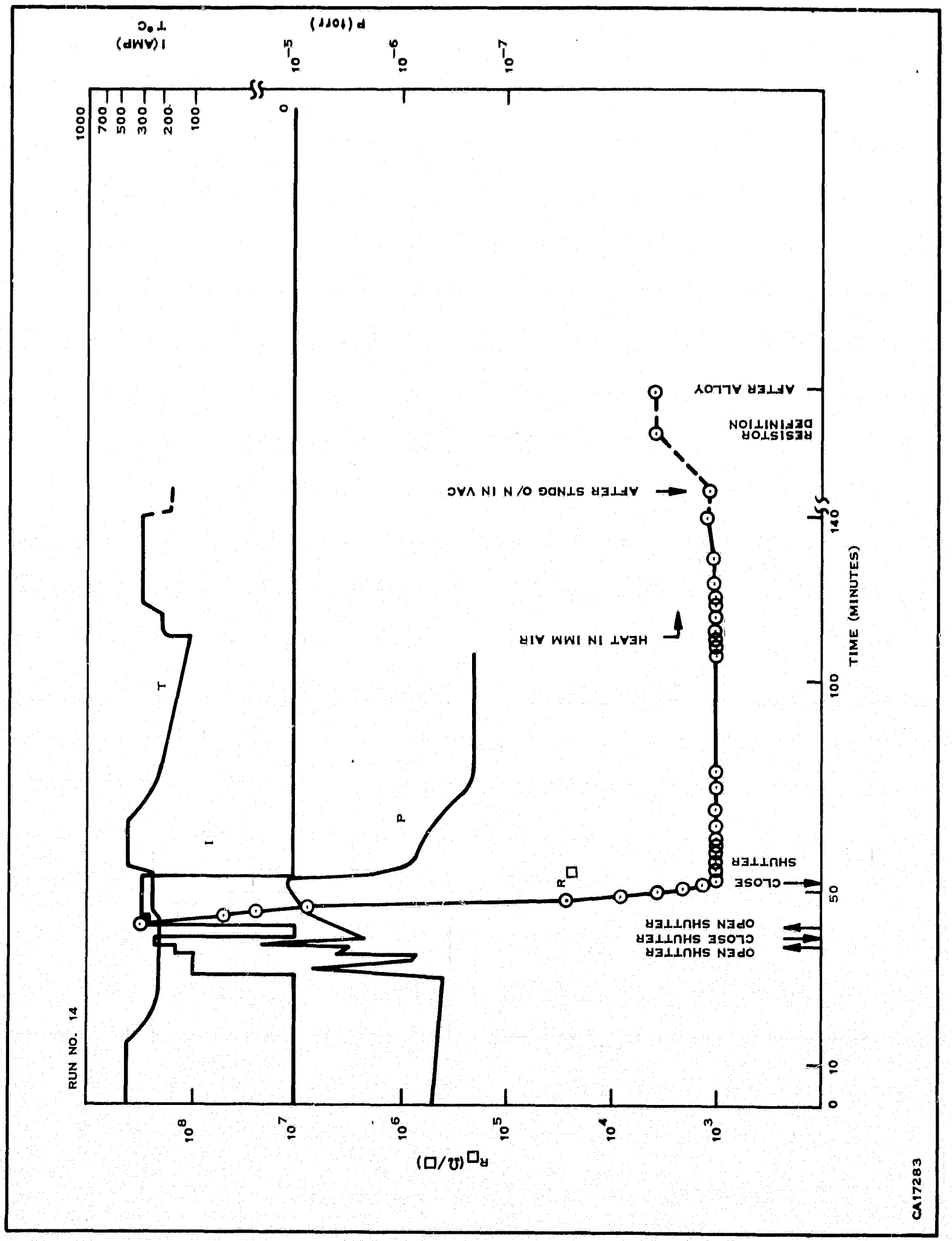


Figure 52. Deposition Conditions — Run Number 14

$M_{14} = 123$ mg

$M_{11} = 386$ mg

Inserting these values

$$\frac{t_{14}}{t_{11}} = 0.537$$

Using the electron microprobe value of 1035Å for average thickness for Run No. 11, the estimated film thickness for Run No. 14 is

$t_{14} = 555$Å

whereas the microprobe value was 340Å.

Run No. 15. Figure (53)

The aim of this run was to duplicate the air age stability obtained in Run No. 14, but at a higher sheet resistance of 3000 ohms/square. A fresh charge of 132 mg was added to the depleted charge of Run No. 14. Extra care was observed to minimize outgassing which again necessitated a two stage deposition. In the first stage, resistance deposition was achieved in 1 minute at 250 amp probably due to lower vacuum where less chromium oxidation occurred. In the second deposition stage, pressure was again maintained below 10^{-5} torr. The resulting film is seen to be much more stable with regard to air age effects and the resistor definition operation. Another unique feature of this deposition is the very high SiO content, 71.5 at %, of the film. A 6-minute deposition at 1215°C would normally result in a 48% film, so it would again appear that filament temperature is primarily responsible for the film composition. It was noticed that the lower boat was poorly attached to the top heater strip, which could possibly account for the lower temperature.

Run No. 16. Figure (54)

The charge residue from Run No. 15 was carefully removed from the tungsten boat and replenished with a fresh charge of 99 mg. mass. The objective in this experiment was the deposition of 5000 ohms per square in a high vacuum. As can be seen from Figure (54), the deposition rate was extremely rapid. After 1.5 minutes at 275 amperes with shutter closed, the first 275 amp deposition took only 1 minute to reach 1.6×10^{5} ohms/square. The second deposition required only 2 minutes to reach 5000 ohms/square while pressure remained at or below 1.8×10^{-6} torr. Electron microprobe analysis indicates a chromium rich deposit containing only 8.2

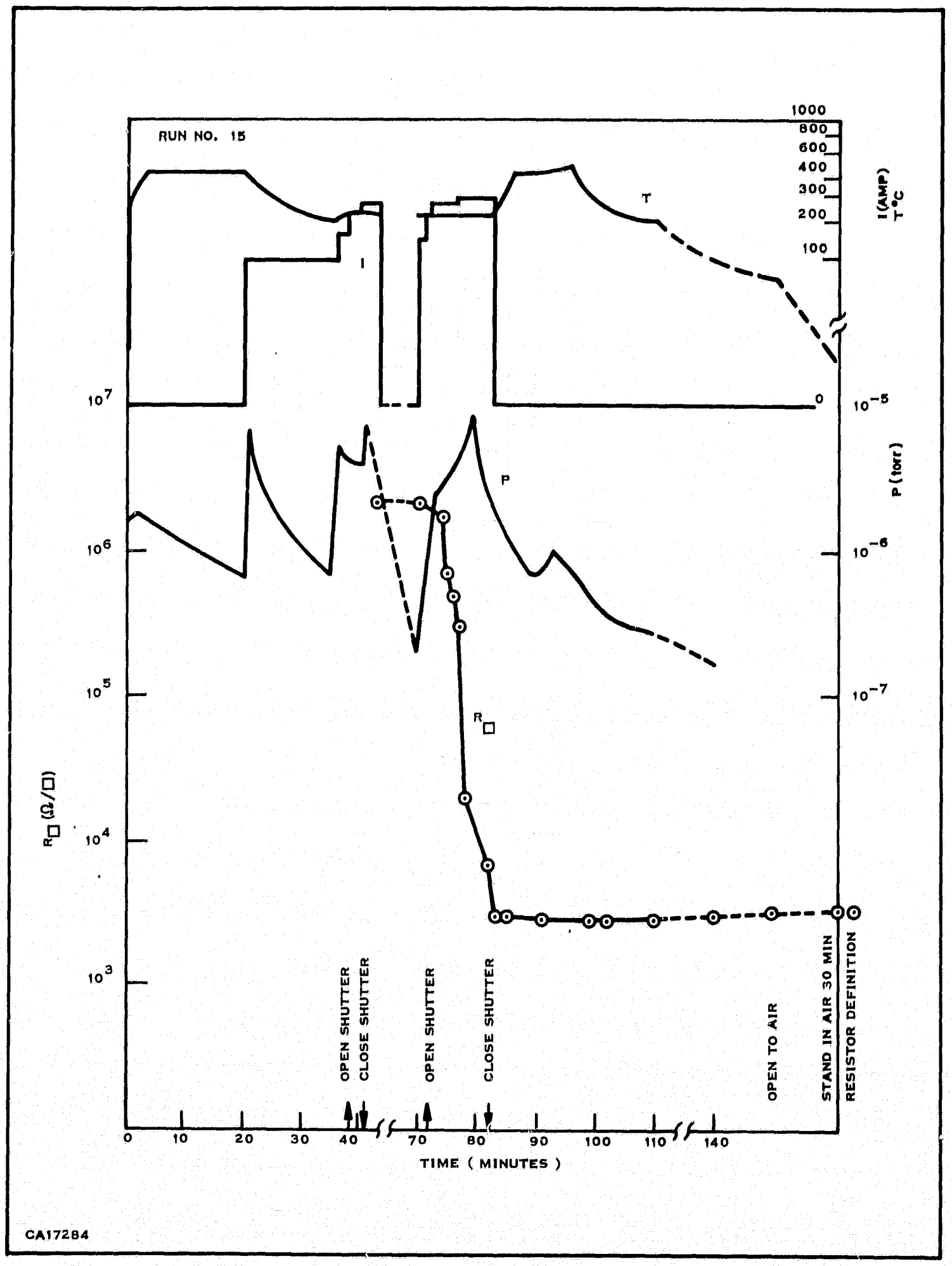


Figure 53. Deposition Conditions — Run Number 15

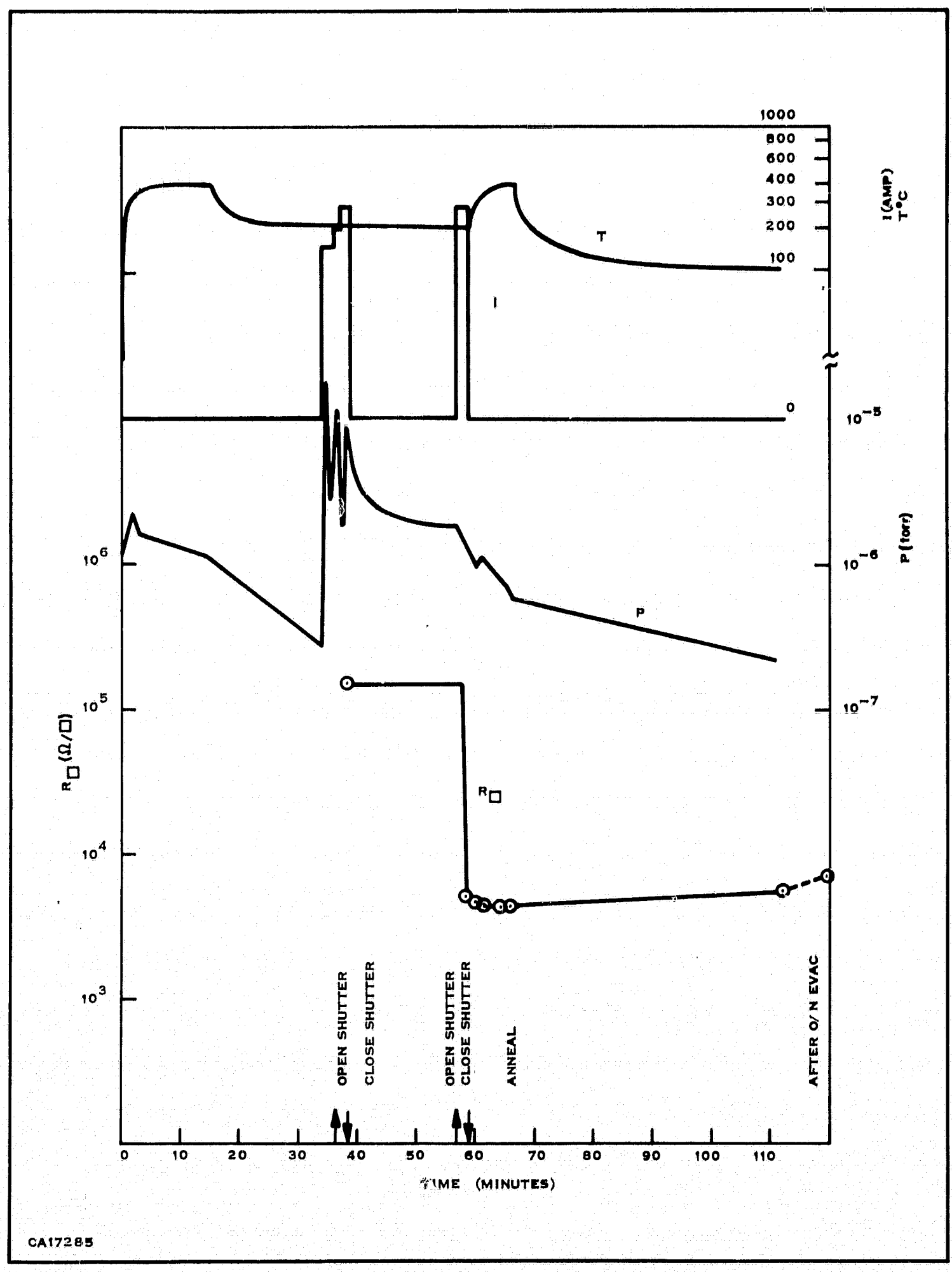


Figure 54. Deposition Conditions — Run Number 16

atomic % SiO. Figure (36) shows a cumulative deposition curve for 1310°C with preliminary shutter closure of 1 minute. A 1.5 minute closure would lower the curve still further. Thus at 4.0 minutes the SiO content is 9.0 at % SiO or less, in excellent agreement with the measured value. The low value of 50 Å obtained for the film thickness is difficult to predict for the 1310°C filament temperature condition. The Time of Flight deposition rate data is quoted in arbitrary units which bear no relationship to each other at the different temperatures. However, it would be valid to observe that a low value of thickness would be expected since a major fraction, about 60%, of the SiO is deposited in the 1.5 minute shuttered sequence (Figure 36). In Figure (37) we see that at the end of this period the cermet being deposited contains 15.0 at % SiO, decreasing rapidly to 8.5% one minute after exposure. Consequently we do not expect the film to be a thick composite of a sublayer of high SiO content superimposed by a thick chromium rich layer but rather a thin, SiO deficient film throughout.

The previous discussions of Runs 11 to 16 have not mentioned the subject of film resistivity. In Figure (20) resistivity in micro-ohm-cm is plotted versus film content in atomic percent of SiO for the films as deposited, as well as calculated resistivity values after air age and resistor fabrication alloy. For comparison, results quoted in the literature are also shown. The only results (representative) of a simple evaporative deposition technique similar to the one described in this report are those of Pitt, [30] who did not analyze film composition. The range of resistivity values which he obtained are shown on the left of Figure (20). and agree with those obtained at Texas Instruments. Considerably different resistivity versus composition dependence is shown in the data of Glang, Holmwood, and Herd (flash evaporation), Braun and Lood (flash evaporation) and Lood (co-evaporation). On the basis of the models proposed by Glang et al and Lood, Cr, Si, Cr_3Si, SiO, SiO_2 and possibly Cr_2O_3 exist in varying degrees of concentration, crystallization and dispersion (Sections III A-3). The Plateau in Figure (20) is attributed to formation of conducting Cr_3Si which bridges metallic islands of Cr. The data of Lood and of Ostrander et Lewis, who both used co-evaporation techniques agrees in part with the flash evaporated data. It is not apparently possible to interpret differences in behaviour on the basis of slice temperature and hence thermally enhanced Cr_3Si formation during deposition, at temperatures which vary from 200°C to 400°C in the references quoted. The most likely factor influencing the resistivity-composition behaviour is metallic particle size and dispersion in the deposited films. The onset of high resistivity at SiO concentrations in excess of 30 at % (Ostrander and Lewis) [32], and the semi-logarithmic dependence and high values seen by Beckerman et al [31] and

Miller et al [40] point to isolated metallic islands in an insulating matrix with electrical conduction dominated by tunneling. This is very different from the concept of Cr_3Si bridging between the islands. The results obtained at Texas Instruments follow an entirely different behaviour where resistivity shows far less dependence on composition. Below 40 atomic % SiO it might be said some plateau formation exists, but it is meaningless to infer Cr_3Si formation since the resistivity is up to one order of magnitude higher. A possible interpretation of this behaviour is that insulated metallic island formation dominates at the lower SiO concentrations. At higher concentrations, chromium rich top layers are formed, effectively shorting out the insulating lower regions. Furthermore, electronic transport in very thin layers is dominated by surface scattering, lowering effective carrier mobility. This behaviour would logically account for the apparently low values of resistivity of film with high SiO content, and would furthermore be characteristic of a non-uniform deposition process such as simple evaporation of Cr-SiO mixture. Again, it should be pointed out that Pitt obtained film resistivity values extending over an almost identical range.

Another striking similarity between the results of Pitt[30] and this contract is the effect of air age on film sheet resistance, Figure (55). Pitt did not specify the conditions of air age. However, our observations are that this is a fairly rapid phenomenon in susceptible films, with most of the resistance increase occuring within 10 minutes at room temperature. Although Pitt's values of film sheet resistivity extend over a smaller range and our data shows considerable scatter, the similarity in air age behaviour is evident and appears to be characteristic of this type of deposition. It is surmised that resistance increase on air age is due to oxidation of the surface chromium. There is some evidence that indicates greater susceptibility to air age when deposition occurs in poor vacuum, where the deposition time is lengthened due to oxidation of chromium in the charge. If resistor deposition is achieved under these circumstances, the final layers would be excessively Cr-rich and hence thin and more prone to oxidation.

Resistance increases observed during the resistor pattern definition operation are not understood. The operation is a wet type, carried out at room temperature. Examination of defined patterns and resistances of different geometries does not indicate poor definition as the cause. Resistance increases occurring during the alloy and bonding operations are more readily reconciled with oxidation effects, as in air aging.

The behaviour of sheet resistance at different stages in the processing sequence is depicted in Table (12) for all the deposition runs performed under this contract.

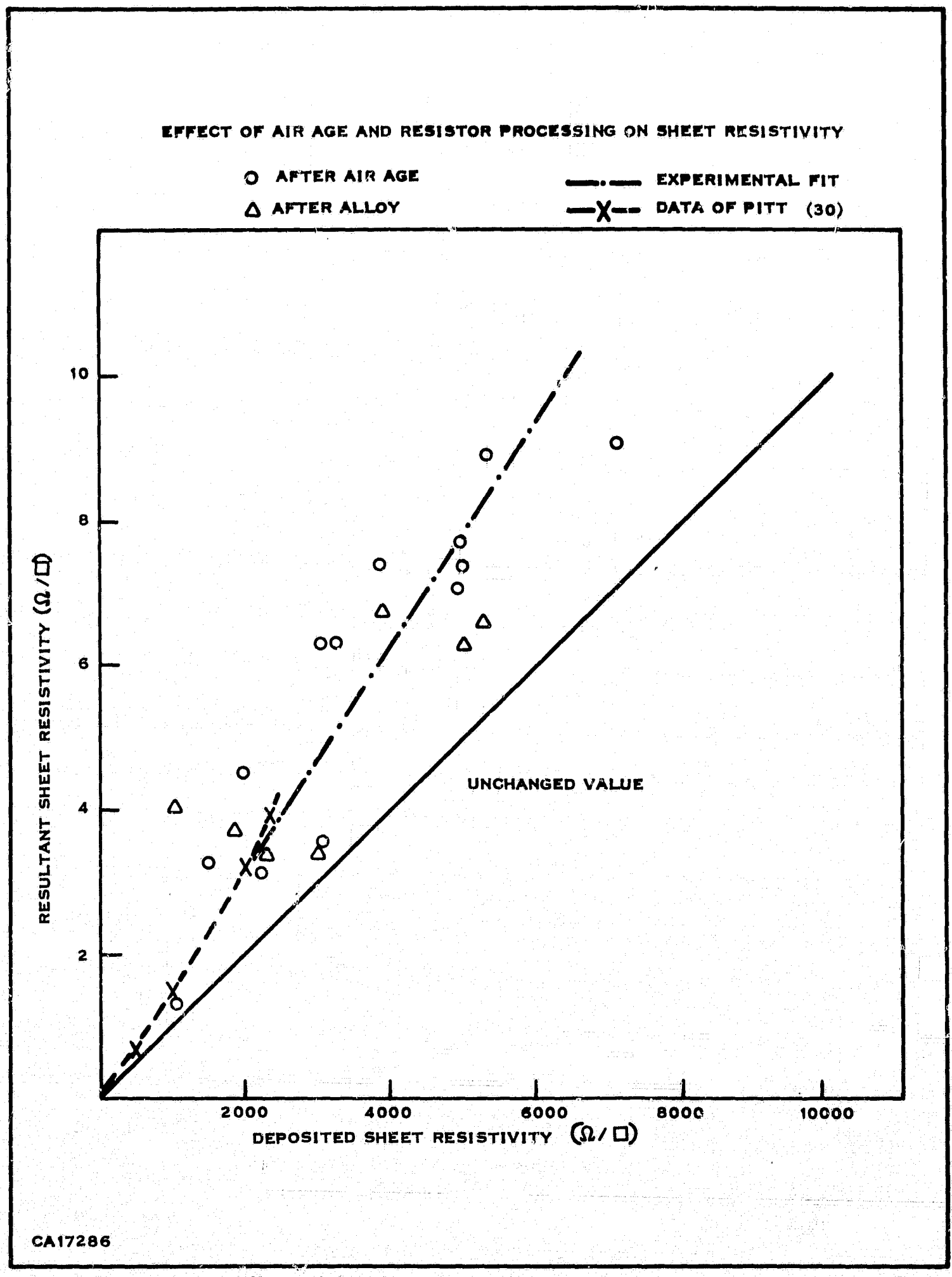


Figure 55. Effect of Air Age and Resistor Processing on Sheet Resistivity

Table 12. Process Sequence Dependence of Sheet Resistance

Run #	$R_{\square}$ At Deposition	$R_{\square}$ Annealed	$R_{\square}$ After Exposure To Air	$R_{\square}$ After Resistor Definition	$R_{\square}$ After 400°C VAC Alloy
7	5100	11,500	20,000	—	—
8	16,800	65,500	11,900	—	—
9	1600	1990	3200	—	—
10	2000	3600	4500	—	—
11	2220	2700	3140	3860	3440
12	5300	6250	8900	6430	6580
13	7150	—	9100	10,000	—
14	1032	1042	1350 After 300°C In Air	4000	4000
15	3140	3140	3520	3750	—
16	5050	5620	7350 After Overnight in Rough vacuum	—	—
17	4780	6580	7150	58,000	73,000
18	3340	5700	6250	22,700	—
19	3050	3720	6250	3360	3400 4400*
20	5000	5000	7700	5980	6250
21	3950	3455	7380	7550	6700 8600†
22	1970	Not Annealed	—	4100	3710 5300*

*After Device Fabrication
†After 550°C 30 min Alloy in N_2.
Sheet Resistance, $R_{\square}$, in ohms per square

Shown are: sheet resistance values observed at the time of deposition; after vacuum annealing at 400°C for a typical period of 5-10 minutes; after occurrence of air age; after resistor definition and before contact alloy; and finally after contact alloy, which typically is performed at 400°C under vacuum except where noted.

The following comments pertain to runs in Table (12) not fully covered in other sections of this report.

Run No. 7:

This was the first of the cermet deposition runs. Charge mass used was 73.2 gm in a clean fired boat system. Filament temperature was raised slowly every 2-3 minutes in a series of twelve current increments to 240 amperes where it was maintained for 16 minutes and then raised to 250 amp for 8 eight minutes. At higher current levels the pressure remained high, 0.8 to 2 x 10^{-5} torr, and resistor deposition rate was slow, requiring 24 minutes to deposit to 5000 ohms per square. Considerable air ageing was observed. It was considered from the observed behaviour that filament current could be raised more rapidly, in fewer steps, to achieve outgassing without SiO deposition, and also that filament current should be raised to 275 amperes to achieve more rapid deposition.

Run No. 8

Deposition parameters are shown plotted in Figure (56). The purpose of this and the two following runs was to investigate whether the Cr-SiO charge tends towards an equilibrium condition with use. If so, this would provide uniform film composition and more controllable deposition governed only by overall charge depletion. Since films of approximately 5000 ohms per square were desired, a small charge mass (73 mg) was used to accelerate the process.

Note that with the prolonged 275 ampere heating, outgassing was severe and resistor deposition very slow; this was later interpreted as due to chromium oxidation. Film thickness deposited 500 Å with resistivity 8.4 x 10^{4} micro-ohm-cm. Note also the extensive air ageing, which also occurs in a partial vacuum (sealed Bell jar) storage overnight. Resultant resistivity was 6.0 x 10^{5} microhm-cm.

Runs No. 9 and No. 10

These runs were made sequentially using the depleted charge from Run No. 8. The rate of resistor deposition slowed down drastically with time, each deposition took over twenty minutes and was accompanied by severe outgassing (P = 3 x 10^{-5} torr), during production of 2 — 4 x 10^{3} ohms per square. The resulting films were highly

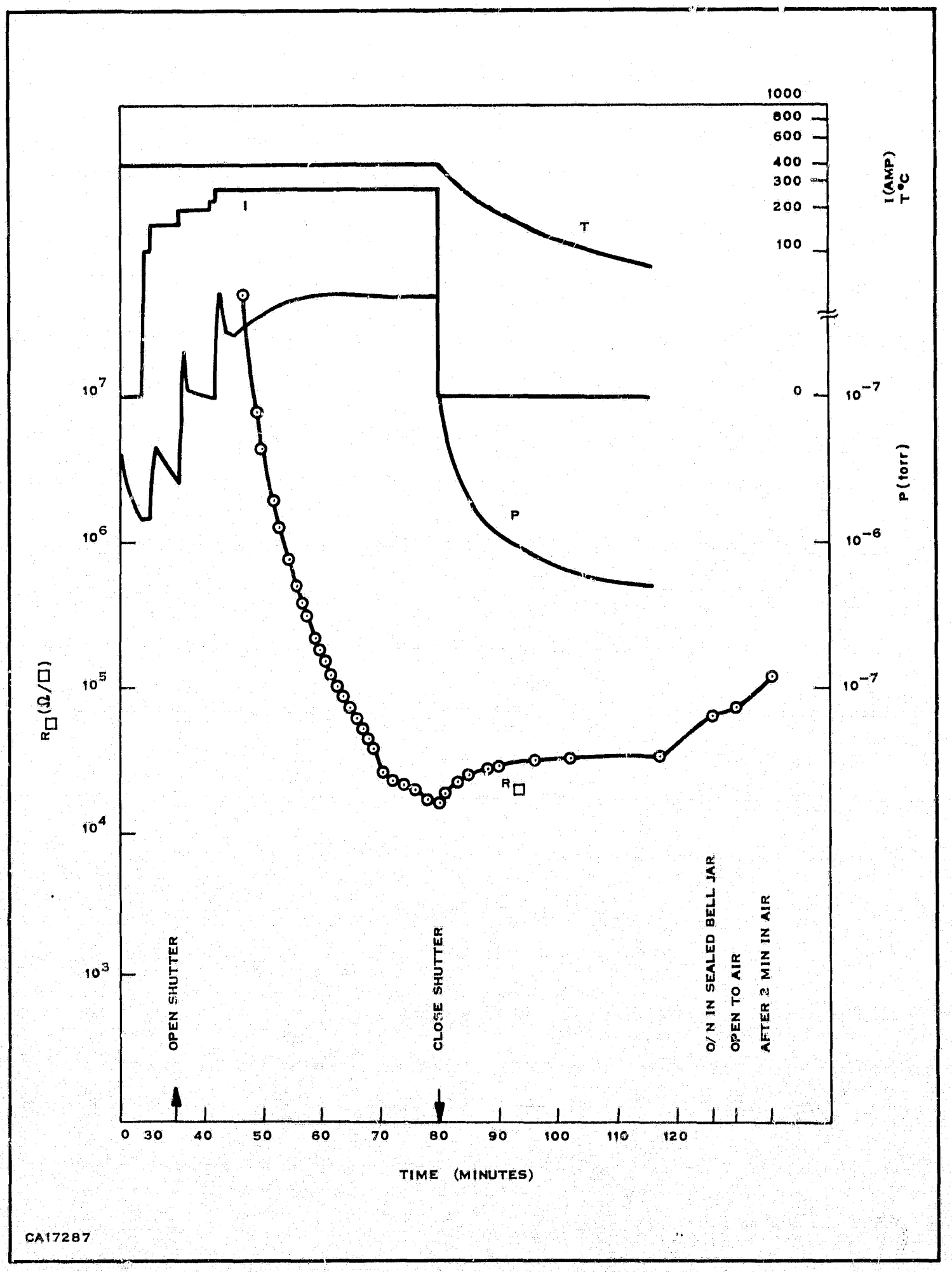


Figure 56. Deposition Conditions — Run Number 8

susceptible to oxidation effects with Run No. 10 exhibiting resistance values of about 3.0×10^{9} ohms per square after the resistor definition operation.

Runs No. 17, 18

The purpose in both these runs was elimination of the uncertainties of annealing phenomena by deposition at 400°C. The depositions in themselves were fairly typical, with some air ageing occurring. However both runs yielded extemely high resistor values after the resistor definition operation, in the range of 30,000 to 60,000 ohms per square before and after contact alloy. The reason for this behaviour is not understood, especially since successful depositions at these temperatures have been reported by Braun and Lood [13], followed by photolithographic resistor definition operations.

Run No. 19

This was an attempt to duplicate the excellent stability observed in Run No. 15, to the extent of adding 162 mgm of fresh charge to the depleted charge of Run No. 18. Outgassing was kept below 7×10^{-6} torr by splitting the run into two depositions of similar total duration to Run No. 15. Air ageing increase, of the order of 100%, however, was present in contrast with almost none in Run No. 15. These effects, combined with those of definition, alloying, mounting and bonding resulted in a final resistivity value of about 4400 ohms per square, well within the 5000 ± 20% range required to satisfy the contract. In view of the encouraging behaviour of this group, devices from this run were selected for TCR evaluation, stress test, noise evaluation and submission to the agency in accordance with the terms of this contract.

Runs No. 20, 21 and 22 were essentially attempts at duplicating Run No. 19 with varying degrees of success. Pressure was maintained below 10^{-5} torr during deposition, which was fairly rapid in all cases. Film thickness and resistivity for Run No. 20 was 418 Å and 2.5×10^{4} microhm-cm respectively, and for Run No. 22 was 345 Å and 1.20×10^{4} microhm-cm after the resistor definition operation. Lack of fine resistance control is evident.

G. EXPERIMENTAL: STRESS TEST RESULTS ON CERMET RESISTORS

The supplemental agreement to the contract called for a thermal stress test of the cermet resistors at a temperature of 175°C for 271.5 hours. Since no current was specified, it was decided, with the approval of the contracting authorities, to subject units to a load current of 10 microamperes for a period of 168 hours. This current level corresponds to circuit load conditions. Some of the units were followed by a

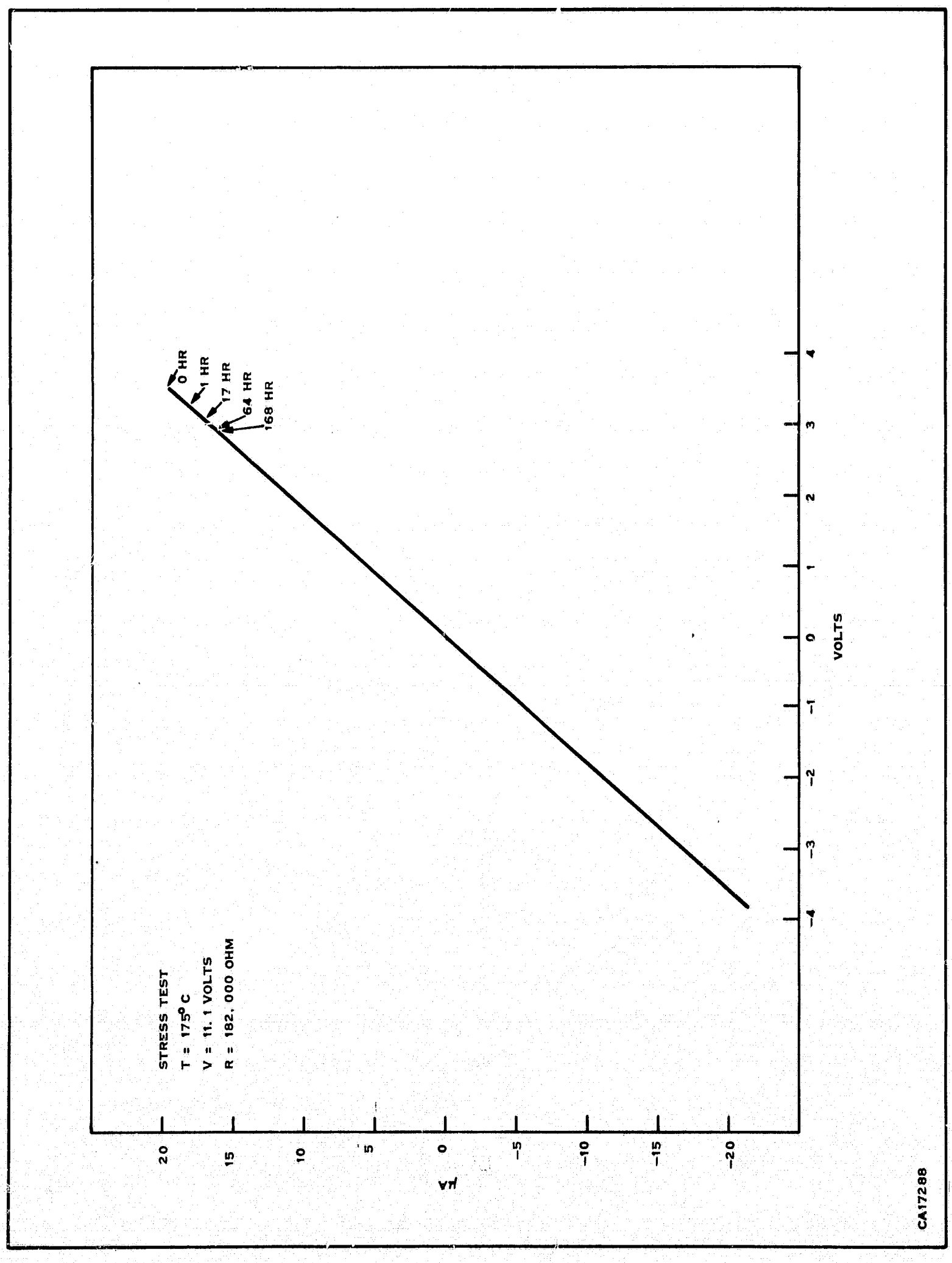


Figure 57. Stress Test Stability

further 168 hour test with a nominal load current of 67 microamperes. Resistance was evaluated by a direct x-y plot of current vs voltage, for both positive and negative voltage magnitudes up to about 3.5 volts. No instability was observed within the limits of resolution of the measurement, which was approximately ±0.5%, due to possible errors in pen location, pen width and multiple retracing. However this is an acceptable error range in view of the 20% tolerance called for in the contract. A typical trace obtained is shown in Fig. (57). All other traces appear almost identical, except for the value of the resistance which is reflected in the slope. These are listed in Table (13). Resistance values were measured at exactly the 0, 1, 17, 64 and 168 hour test points.

In the matter of selection of resistors, reference is made to the binary counter chip layout, see Fig. (8). In the 10 microampere load current test (Test #1), 8.5 volts was applied across the 850,000 ohm (nominal) resistor taps, numerically designated 2 and 5. The letter designations A, B, C and D refer to the four resistor legs in each circuit. In the 74 microampere load current test (Test #2), 11.1 volts was applied across the 150,000 ohm (nominal) resistor taps 2 and 3. Table (13) lists the units life tested, and pertinent conditions. It is evident that under these stress conditions the resistors are stable within the limits of resolution prevailing. Under Test #1 conditions 8.5 volts applied across 850,000 ohms generates 0.5 watts/sq. cm. or 3.2×10^{-3} mW/mil^2. In the more severe case, 11.1 volts applied across 150,000 ohms generates 27.5 watts/sq. cm. = 178 watts/inch^2 = 0.18 mw/mil^2. This power dissipation level is less than that reported by Schaible, Overmeyer and Glang[42] but yet considerably greater than that of Beckerman and Thun, [31] see Section (IIIA-4).

H. EXPERIMENTAL: CERMET RESISTOR REPRODUCIBILITY

The factors that affect reproducibility of cermet thin film resistors are primarily: (1) deposited sheet resistance, (2) quality of geometrical definition, (3) contact resistance and (4) ageing and annealing effects. The latter have been discussed in section (III A-5). Experience gained in this study indicate:

(1) for the most part, Al-Cr/SiO contacts have an acceptably low contact resistance. This is readily ascertained by examining resistance of the patterns of Fig. (45), particularly those of width 0.5 and aspect ratios 18, 48, 3 squares, designated L, B and J. The 150,000 (nominal) and 850,000 (nominal) resistance taps of the binary counter circuit have aspect ratios of 33 and 187 squares respectively. With negligible contact resistance, the logarithmic distribution plots should maintain constant relative

Table 13. List of Stress Tested Units

Device #	Connection Test #1	Measured Resistance (Kilohms)	Test #1 Stress Current (Microamperes)	Connection Test #2	Measured Resistance (Kilohms)	Test #2 Stress Current (Microamperes)
1	2-5	910	9.3	2-3	160	69.4
2	2-5	508	16.7			
3	2-5	1015	8.4	2-3	182	61.0
4	2-5	840	10.1			
5	2-5	848	10.0			
6	2-5	950	8.9	2-3	159	69.9
7	2-5	850	10.0	2-3	152	73.0
8	2-5	964	8.8	2-3	169	65.7
9	2-5	812	10.5			
10	2-5	952	8.9	2-3	172	64.6

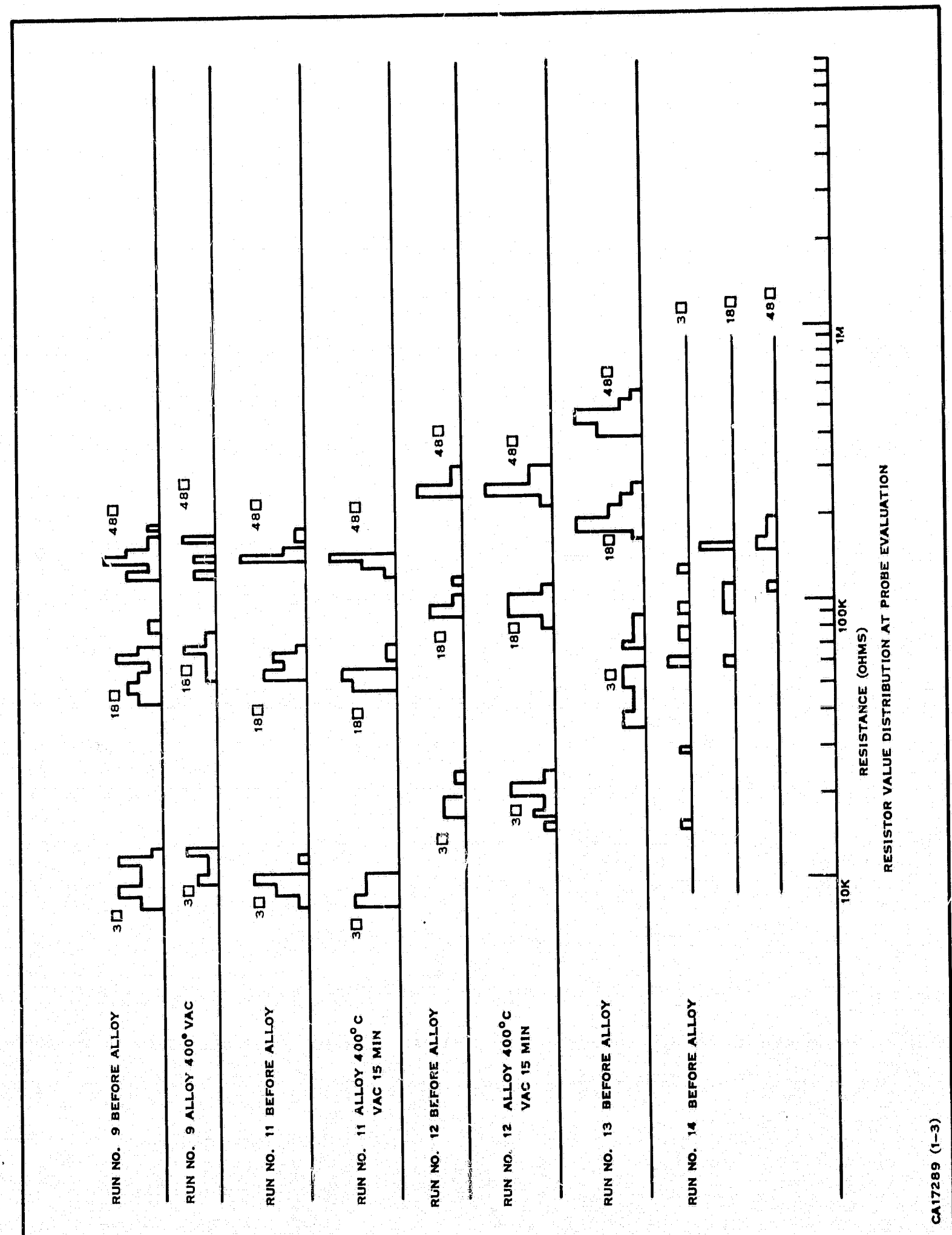


Figure 58. Resistor Value Distribution at Probe Evaluation Sheet 1 of 3

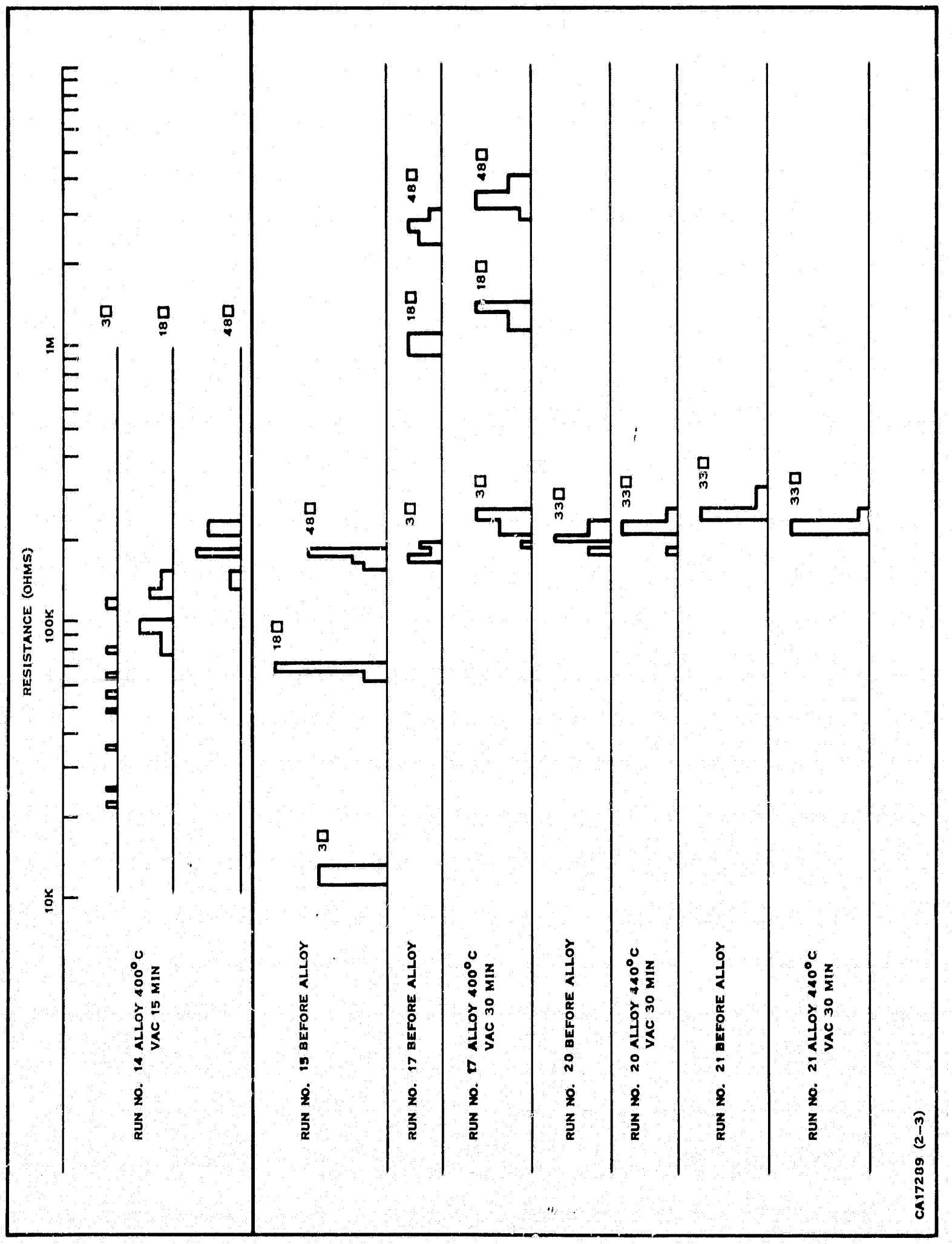


Figure 58. Resistor Value Distribution at Probe Evaluation Sh

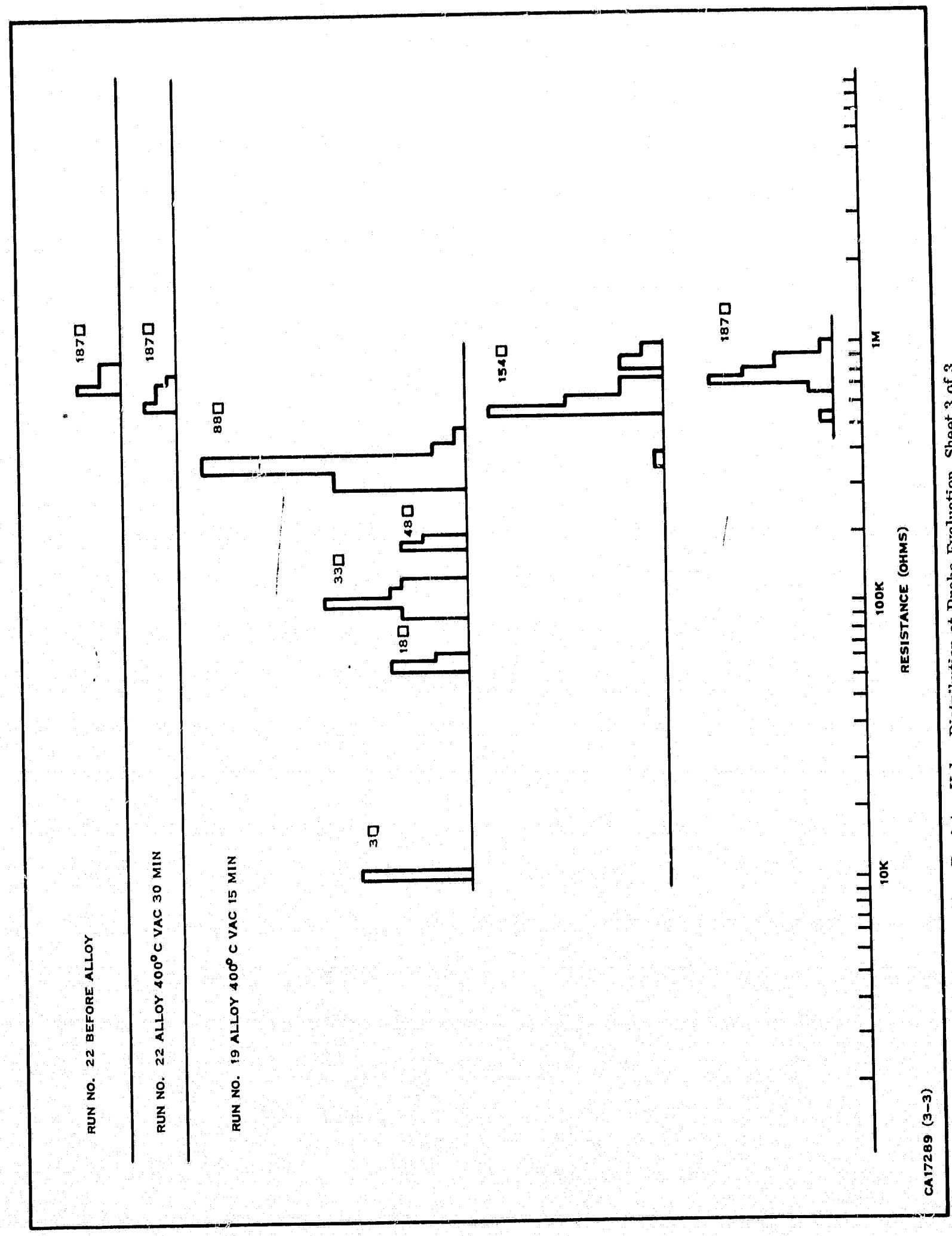


Figure 58. Resistor Value Distribution at Probe Evaluation Sheet 3 of 3

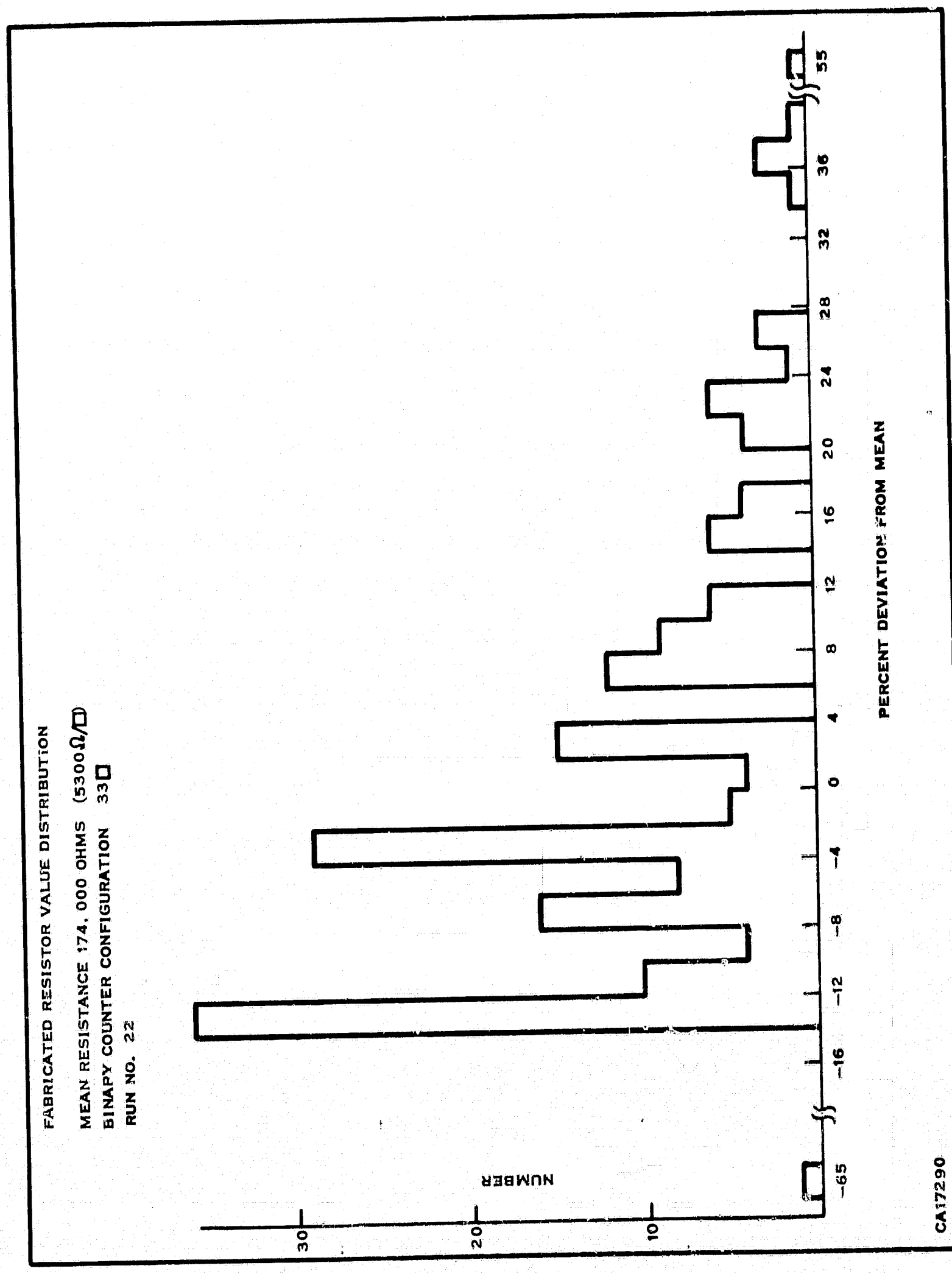


Figure 59. Fabricated Resistor Value Distribution

positions irrespective of sheet resistance. Fig. (58) shows most of the runs had satisfactorily low contact resistance except runs #13 and #14. In Run #13, configuration J (= 3 squares) should have resistance values centered at around 35,000 ohms. It is evident that contact effects resulted in higher resistance values with a larger spread. It should be noted that for the most part aluminum contacts to Cr-SiO cermet films have an acceptably low resistance in the as-deposited condition and show little or no change in the alloying operation which is usually 400°C in vacuum for 15 to 30 minutes. The behavior of Run #13 might be explained on the basis of the presence of a top layer of SiO, discussed in Section (III F-3). In the same section, it will be recalled that Run # 14 was deposited to 1000 ohms per square, followed by an oxidation cycle. The 30% increase in monitor resistance value was very likely achieved by oxidation of the top chromium layer to insulating Cr_2O_3, preventing a low resistance top contact.

(2) In this study only one technique of geometrical definition has been used, namely that of the reverse aluminum process. Examination of Fig. (59), which is representative of 185 resistors fabricated on the same slice (Run #22-5), suggests that width variations exist, but on the side of increased rather than lower resistance. The units measured were not pre-selected but have a genuine sharp cut off as indicated. The extent of the scatter of resistance values is comparable to that obtained by Pitt[30] using a similar deposition process. The data of Fig. (59) shows that 84% of the resistors fall within ±14% of the arithmetic mean value, and 34% fall within ±6%. Note that this is for assembled, canned units. This distribution is more scattered than that obtained in the pellet flash evaporation technique of Glang, Holmwood and Maissel[34]. However, they do not specify sheet resistance values in their distribution data, but from the test it appears to be around 50 ohms per square. Low values like this help to reduce scatter. The powder flash evaporation data of Braun and Lood[29] in Fig. (18) shows a ±10% scatter for 1-mil wide cermets and an average deviation of ±1.8% for non-adjacent resistors on the same chip. For 0.5 mil wide resistors this figure increases to ±2.5%. Our data in Fig. (59) is for 0.4-mil geometry, with non-adjacent deviations averaging ±0.8% for resistors on the same chip, which indicates considerably better close range reproducibility.

Evaluation of resistor value distributions was performed on a majority of the deposition runs described in this report. This was done by probing across two diagonals of a slice at right angles to each other. The resulting data is plotted in histogram form in Fig. (58). It will be seen that for each particular resistor configuration and run, the scatter is generally within ±20% limits. On the basis of the

above data, one can infer that this scatter is primarily due to sheet resistance variations across a slice. Contact resistance and geometry variations play a secondary role with the techniques used here. The sheet resistance variations are primarily due to compositional fluctuations affecting bulk resistivity and annealing behavior, points which have been fully discussed earlier in this report. (See Section III A-3). The spread of resistor values seen from run to run is also due to the same basic cause: lack of compositional control. The similar results obtained in this study and by Pitt[30] indicate that this problem is a basic defect of this method, indeed in most of the techniques studied by others. At the present moment the best results have been reported for the pellet flash evaporation method of Glang, Holmwood and Maissel. However, little has been reported on sputtered cermet films, which may be a fruitful area of study.

I. EXPERIMENTAL: CERMET RESISTOR NOISE

Several units have been proposed to express the current noise of resistors. The unit of microvolts per volt as designated in the JAN-R-11 Specification has been in use for some time but suffers from unreliability due to dependence on the condition of the test gear. Furthermore the unit cannot readily be used to estimate the noise that a particular resistor will introduce in an electronic circuit. The conversion gain technique is capable of overcoming the above problems. More recently the Noise Index has been proposed as a noise unit that is readily usable for circuit noise calculations. The technique is as specified in MIL-STD-202B dated 14 March 1960, described as Method 308, Current-Noise Test for Fixed Resistors. The equipment used was the recommended Model 315 Resistor-Noise Test Set made by Quan-Tech Laboratories, Inc.

In the following we use the Noise Index expressed in db as a measure of current noise. Values for freshly fabricated (bonded in hermetic can) cermet resistors are shown in Table (14) as measured at various applied voltages from 50 V up to about 200 V. For comparison, Noise Index values are also shown in Table (14) for metal film, and carbon film resistors. It will be seen that the carbon variety is considerably more noisy than either metal film or cermet. The cermet resistors appear to be more noisy at the higher voltages than metal films, but for practical purposes are quiet, with noise values generally below -10db; the uncertainty is due to the high system noise of the test instrument. A quieter instrument indicated noise values of -17 db, corresponding to 0.14 microvolts per volt in a frequency decade. This is higher than results obtained by Pitt [30], 0.07 μV/V for 2500 ohm/sq. resistors, who showed that increasing sheet resistance results in higher noise. The devices measured under this contract

Table 14. Comparison of Noise Index of Cermet, Metal and Carbon Resistors

Resistor No.	Resistance (Ohms)	Applied Voltage		System Noise S (db)	Total Noise T (db)	Noise Index I	Remarks
		V (volts)	D (db)				
CM 11	179 K	50.0	34.0	23.2	24.0	-17.4	CERMET
CM 12	179 K	50.0	34.0	23.2	24.6	-14.8	CERMET
CM 13	181 K	50.0	34.0	23.2	24.6	-14.8	CERMET
CM 14	195 K	50.0	34.0	23.8	25.5	-13.3	CERMET
CM 15	179 K	50.0	34.0	23.2	25.0	-13.6	CERMET
CM 15		100.0	40.0	23.2	29.8	-11.3	CERMET
CM 15		200.0	46.0	23.2	46.5	+ 0.4	CERMET
CM 16	175 K	50.0	34.0	23.0	24.8	-13.8	CERMET
CM 16		100.0	40.0	23.0	28.2	-13.4	CERMET
CM 16		200.0	46.0	23.0	37.5	- 8.6	CERMET
CM 17	195 K	50.0	34.0	24.0	25.2	-14.8	CERMET
CM 17		100.0	40.0	24.0	28.5	-13.4	CERMET
CM 17		200.0	46.0	24.0	37.0	- 9.3	CERMET
CM 18	170 K	50.0	34.0	23.0	25.5	-12.1	CERMET
CM 19	168 K	50.0	34.0	23.0	24.5	-14.7	CERMET
CM 20	170 K	50.0	34.0	23.0	25.2	-12.8	CERMET
MF 1	115 K		25.9	19.5	20.0	-15.1	METAL FILM
MF 1		100.0	40.0	19.5	20.2	-31.8	METAL FILM
MF 2	1000K	50	34.0	37.2	37.2	<-10.0	METAL FILM
		200	46.0	37.0	38.2	-13.8	METAL FILM

Table 14. Comparison of Noise Index of Cermet, Metal and Carbon Resistors (Cont)

Resistor No.	Resistance (Ohms)	Applied Voltage		System Noise S (db)	Total Noise T (db)	Noise Index I	Remarks
		V (Volts)	D (db)				
MF 3	1000K	50	34.0	37.2	37.2	<-10.0	METAL FILM
		200	46.0	37.0	38.2	-13.8	METAL FILM
MF 4	1000K	50	34.0	37.2	37.2	<-10.0	METAL FILM
		200	45.8	37.0	38.0	-14.4	METAL FILM
MF 5	1000K	50	34.0	37.2	37.2	<-10.0	METAL FILM
		200	46.0	37.0	38.2	-13.8	METAL FILM
CF 1	909K	16.2	24.3	36.0	37.0	+ 6.1	CARBON FILM
		50.0	34.0	36.0	42.0	+ 6.8	CARBON FILM
		195.0	45.8	36.0	49.5	+ 3.5	CARBON FILM

had a sheet resistance of 4000—5000 ohms per square, which may account for the higher noise index value.

J. EXPERIMENTAL: CERMET RESISTOR POWER CAPABILITY

On the basis of burnout tests, the short term power handling capability of thin film cermet resistors is high. Increasingly large d. c. voltages were applied for periods of 5 minutes at a time to five test resistors with the following values: 178 KΩ, 179 KΩ, 180ΩK, 200 KΩ and 840 KΩ. Voltages were applied in increments of 20 volts. The first noticeable change in resistance occurred at 390 volts. The initial and final resistance values are shown in Table (15). No measurable resistance change was observed at intermediate voltages.

Examination of the burned out unit shows degredation at the gold wire aluminum pad bond suggesting a gold-aluminum compound formation at the elevated temperatures generated. Power dissipation at 400V is 168 mw/mil^2 or 168 kw/inch^2 for the 180,000 ohm resistor used in the binary counter circuit. 400 V applied to the 840,000 ohm resistor generates 6.4 mw/mil^2 or 6400 watts/inch^2. The power handling capacity of the cermet thus appears to be very high. Contact degredation was investigated briefly by studying noise behavior after each increasing power period. Four resistors, each about 180,000 ohms, were studied in this manner using increments of 50 volts. No significant noise increase was noted right up to 350 V. On all four units burnout occurred at 400 volts.

K. EXPERIMENTAL: SUMMARY AND CONCLUSIONS

From the results presented in the literature and the experience gained in this reported study it can be unequivocally stated that controllable cermet resistor deposition is not an easily realizable process. Many methods have been studied and presented in the literature and analysed in this report. The best results to date have been achieved by the pellet flash evaporation process[34]. Sputtering could very well be promising, but has not been thoroughly surveyed in the literature, but is worthy of further investigation.

The method evaluated in this report is, in regard to experimental setup, the simplest, namely that of evaporation from a mixture of Cr and SiO. From the point of view of understanding and of post deposition resistance control, this may be the most difficult system to comprehend, simply because the resulting film is quite non-uniform in composition throughout the depth of the film. This is primarily due to the

Table 15. Resistor Stability Under Increasing Loads

Stress (volts)	Resistor Connections A2-A3 (kilohms)	B2-B3 (kilohms)	C2-C3 (kilohms)	D2-D3 (kilohms)	A3-A4 (kilohms)
Initial	178	179	180	200	840
20	178	179	180	200	840
40	178	179	180	200	840
	Stress applied for 5 minutes in 20 volt increments. No resistance changes observed.				
360	178	179	180	200	840
380	178	190	180	200	840
400	178	195	180	200	840
410	160	open	180	200	830

fact that SiO has a considerably higher vapour pressure than that of chromium; it consequently evaporates more rapidly and as a result alters the composition of the charge from its initial value. This phenomenon has been investigated in detail with a time of flight mass spectrometer; and the resulting time dependences of cumulative film composition have been analysed and found to be highly dependent on temperature, charge mass and time. The literature has shown that post deposition annealing behavior is a strong function of composition. Thus, the non-uniformity discussed above is further compounded by post deposition annealing vagaries. In addition to this, the technique suffers from a post deposition air age effect which in many instances masks the annealing effect by causing a resistance increase. This is attributed primarily to oxidation of surface chromium. The mixture evaporation method is felt to be particularly prone to this behavior because of the postulated oxidation of chromium in the charge itself, reducing the chromium content initially and exaggerating it towards the end of the run by virtue of deposition prolongation, increasing the non-uniformity.

Nevertheless, it is felt that the technique examined in this study is of significance and utility particularly to those experimenters desirous of depositing cermet films with a control accuracy of about a factor of 2 in the sheet resistivity range 2000—5000 ohms per square and who are limited in their resources to the use of a simple, inexpensive apparatus. The similarity of behaviour of the films obtained by Pitt[30] and

those in this study suggest that an empirical target value curve for deposited resistors may be of use. Fig. (55).

Many areas of further study have suggested themselves in the course of this work. The air age effect, which limits adequate control so significantly, may possibly be counteracted by the use of an overcoating of SiO or SiO_2 or possibly some other dielectric, deposited by various means, e. g. sputtering or evaporation. The role of sputtering as a cermet deposition technique should be investigated more thoroughly. The phenomenon of resistance change during the definition as well as the annealing operations should be examined further, as well as in the presence of a protective overcoating. The role of pressure during deposition, apparently influencing charge oxidation and film air aging is also indicated as a fruitful area of further study of non-uniform as well as films of uniform composition.

SECTION IV

MONOLITHIC MNOSFET-CERMET BINARY COUNTER

A. CHIP LAYOUT:

The binary counter circuit specified by NASA is depicted by the schematic in in Figure 60 a. The load resistors were cermet and were bonded to form circuits with 150K, 300K, 600K and 1000K ohms. The terminals bonded to exterior pins for the completed circuits are indicated by the seven numbered boxes.

A topology for this circuit was sought and found in which no p-diffused regions were used for the sole purpose of tunneling under a metal lead. Where tunnels were required, already existing drains or sources were extended to provide the tunnel, minimizing load capacitance. The external lead configuration matching the previous MOSFET circuit was also satisfied by the layout.

The layout of the cermet lead resistors is such that a single set of masks provides circuits having four different nominal values of resistance by ball-bonding to appropriate taps on these resistors. The bonding pads at these taps are connected to the resistors by means of narrow aluminum lines that can be electrically fused (blown out) to remove the capacitance associated with unused pads from the circuit. This was found to be unnecessary because of the very thick oxide under these pads. The conductance of the transistors (width to length ratio) was determined by speed and "saturation" voltage requirements. The speed is limited primarily by the RC time constant of the load resistor and the MNOSFET input capacitance. A decrease in the channel length lowers capacitance while it raises conductance so the minimum length consistent with present technology, 0.2 mils (after, lateral diffusion) was used. A decrease in channel width lowers input capacitance but it also lowers the conductance of the device, raising the saturation voltage. The width used is therefore a performance compromise between speed and saturation voltage. Assuming a threshold voltage of 3 volts, the resistance at the origin of a square ($W/_L = 1$) MNOSFET is about 20 kilohms when the gate voltage is 10 volts. The circuit specification calls for a maximum saturation voltage of 1.5 volts with a 24 k load resistor at $V_{dd} = 10$ volts. The

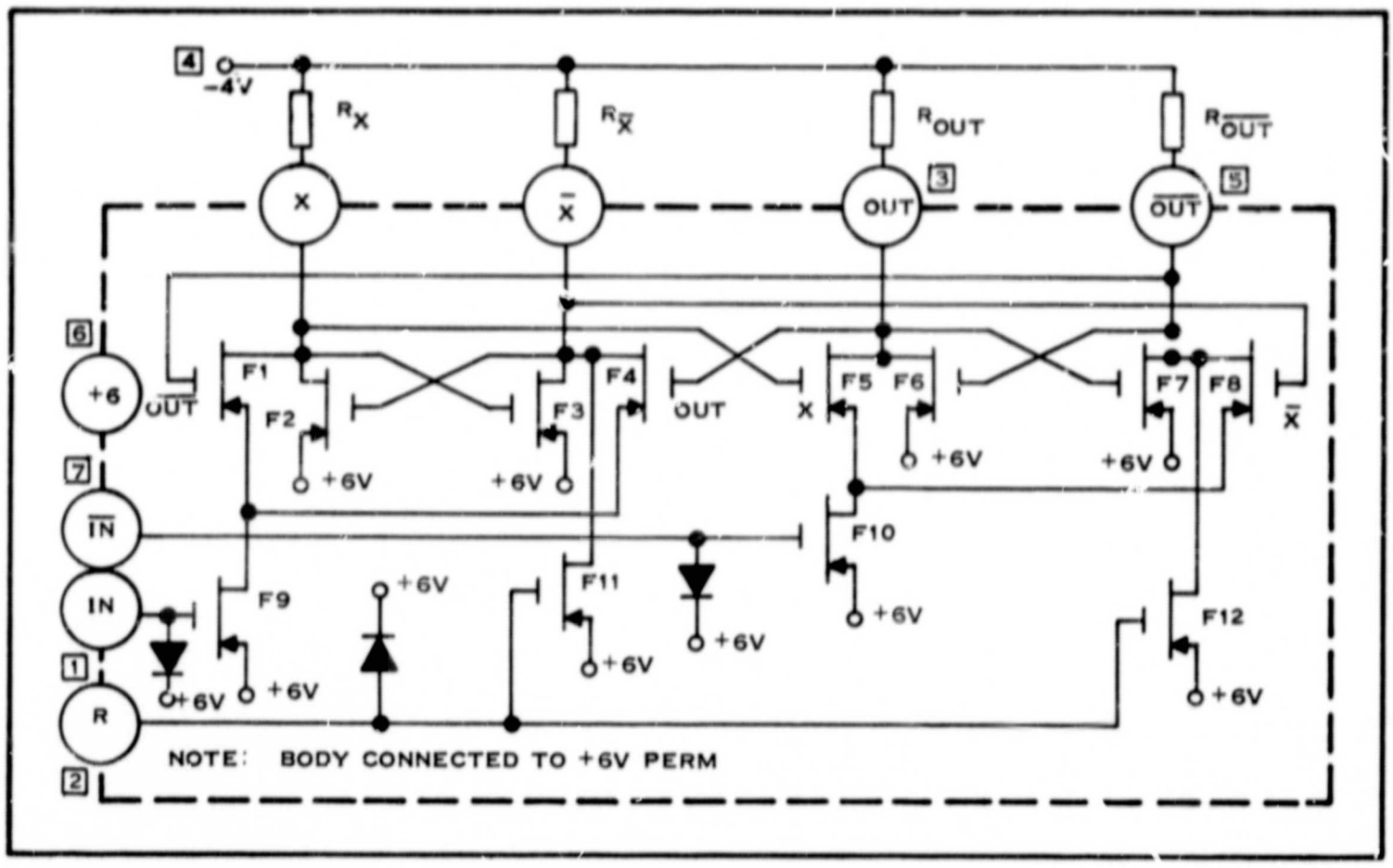


Figure 60. (a) Schematic for NASA Binary Counter Circuit

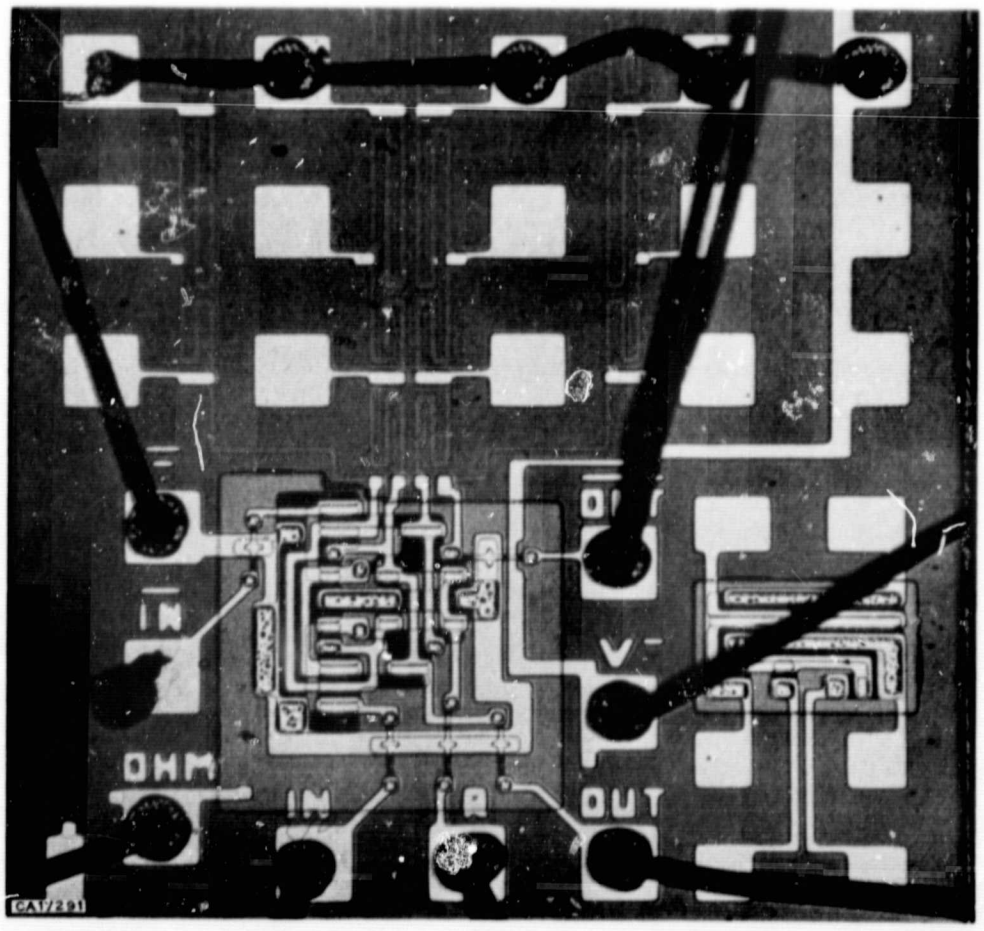


Figure 60. (b) Ball Bonded Binary Counter Chip Configuration Number 4

resistance of the MNOSFET must therefore be $\frac{1.5 \times 24}{10 - 1.5} = 4.2$ kilohms. Thus a width to length ratio of 5 is required, dictating a width of one mil with a channel length of 0.2 mils. When two transistors are in series (F_1-F_5, F_4-F_9, F_5-F_{10}, F_8-F_{10}) the resistance of each must be halved, requiring each to be 2 mils wide. Thus transistors F_2, F_3, F_6, F_7, F_{11} and F_{12} are 1 mil wide and transistors F_1, F_4, F_5, F_8, F_9 and F_{10} are 2 mils wide.

Each of the inputs and outputs are protected against static charge buildup by surface plate avalanch diodes.

B. CIRCUIT PERFORMANCE

The circuits were tested and found to meet or exceed all specifications. The circuit parameter that was optimized in design, speed, far exceeded the requirements. For any given value of load resistance, the circuits performed the binary division at frequencies at least 5 times greater than the specified minimum frequency for that value of load resistance.

There is a requirement on the input voltage waveforms that the input voltage and its compliment do not overlap in the negative direction. Overlap in the positive direction - that is both the input and its complement simultaneously at the most positive voltage - is tolerable. The output voltage waveforms satisfy the requirement of no overlap in the negative direction and one MNOSFET circuit satisfactorily drives another, permitting cascade operation to divide by 2^n where n is any interger.

C. EVALUATION OF DELIVERED UNITS

The Supplemental Agreement to the Contract called for the delivery of ten good circuits, packaged in TO-5 low profile headers. The terms of the contract in this regard have been satisfied with the delivery of ten functioning circuits whose evaluation is discussed in full below. Over and beyond the contract requirements, several units with resistor connections only were delivered for evaluation by NASA.

The ten circuits delivered were characterized by four different groupings of load resistance values. Fig. 8 shows a binary counter chip layout with the resistor taps identified alpha-numerically. Connections A1, B1, C1, and D1 are the small lands near the active region of the chip and are not labelled for clarity. There are four tapped load resistors on each chip. The design of the counter calls for all four of the load resistors used to have similar values, the choice of tap (resistor value) to

be determined by speed requirements and power consumption limitations. The approximate aspect ratio of the different configurations, together with nominal resistor values are shown in Table 16. A sheet resistivity of 4545 ohms per square is required to achieve these values. After a particular value of circuit load resistance is chosen, the appropriate taps are connected together as shown in Fig. 60 and thence to a common strip (column E) connected to the external power supply land (v^-). The four possible load values are characterized in Table 16 as Configurations #'s 2, 3, 4, and 5. Thus the unit in Fig. 60 is described as a configuration #4 unit. Fig.61 shows a chip assembled on a header prior to canning. Pin numbers 1-8 are also shown. The chip is bonded in a #5 configuration. The ten units delivered are as follows in Table 17.

Table 16. Resistor Tap Values

Connections	Aspect Ratio (squares)	R nom (K ohms)	Configuration Designation
A2 - A3	33	150	—
A3 - A4	66	300	—
A4 - A5	88	400	—
A2 - A4	99	450	—
A2 - A5	187	850	—
A1 - A2	33	150	2
A1 - A3	66	300	3
A1 - A4	132	600	4
A1 - A5	220	1000	5

As was mentioned earlier, these units were all fabricated from Run #19, and since a change of resistance was noted during the chip alloy and ball bonding operation, each unit delivered was evaluated for sheet resistivity. Because the resistors are interconnected through p-n junctions in the counter circuit, it was not possible to accurately measure resistor values between the common connection and the circuit. However it is possible to measure from the common connection to all taps external to the circuit, and from this infer the sheet resistivity. In practice the measured

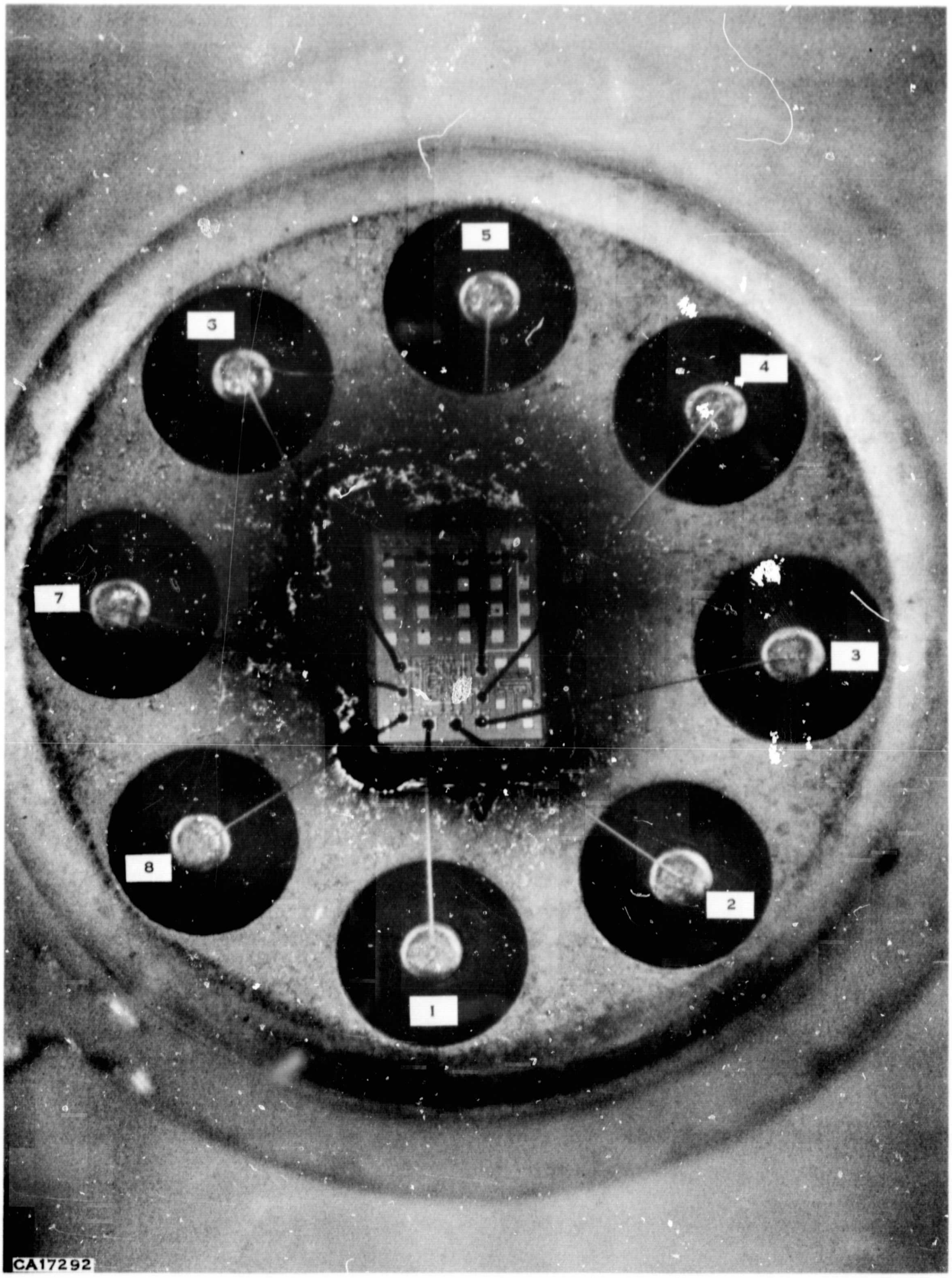


Figure 61. Binary Counter Chips Assembled on Header

Table 17. List of Units Delivered

Unit #s	Configuration #	R nom
1, 2, 7	2	150 K ohm
11, 13	3	300 K ohm
22, 25	4	600 K ohm
34, 35, 36	5	1000 K ohm

resistor values were compared to expected values found in Table 16. The Supplemental Agreement specified an upper limit ±20% of the range of resistor values permissible, on an absolute or ratio basis. These are included together with measured values in Table 18.

Table 18. Measured Resistor Values in Kilohms

Unit #	Bonded Configuration Number	Rnom -20%	Rnom	Rnom +20%	Measured Resistor Connections			
					E-A5	E-B5	E-C5	E-D5
1	2	680	850	1020	690	690	710	800
2	2				750	750	750	820
7	2				750	775	775	810
11	3	560	700	840	580	575	590	625
13	3				580	580	580	650
22	4	320	400	480	340	355	340	375
25	4				355	355	360	380
–	5	Cannot be measured (see text).						

It will be noticed that the "D" resistor leg exhibits consistently higher values than the A, B or C legs. This has been a consistently observed phenomenon throughout all runs and is due to an error in the mask artwork. Close-range reproducibility data mentioned in earlier sections ignored this bias in the distribution. Nevertheless, with this bias included, the values displayed in Table 18 fall within the ±20% specified tolerance range.

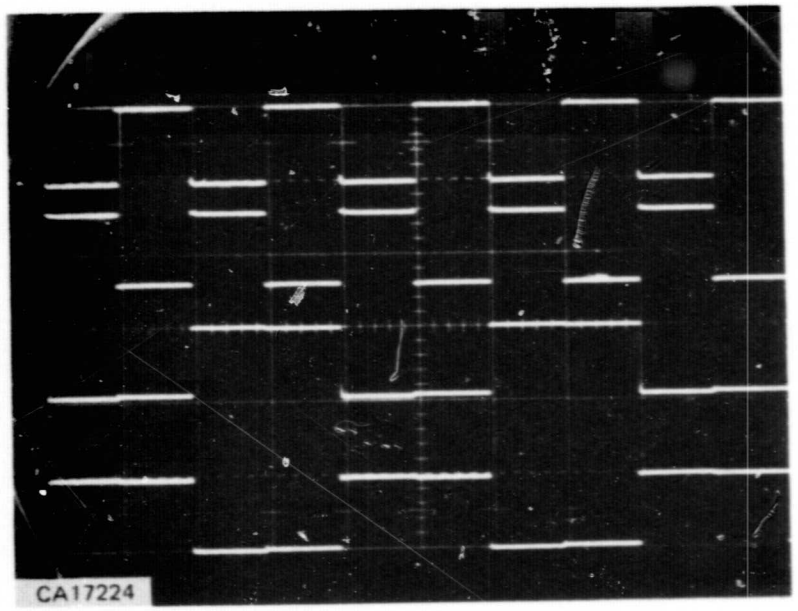
Pin designations are as follows (see Fig 61):

Pin #1	IN
Pin #2	RESET
Pin #3	OUT
Pin #4	V^-
Pin #5	$\overline{OUT}$
Pin #6	GROUND
Pin #7	$\overline{IN}$
Pin #8	OHM

The ten units that were delivered were evaluated for counting performance at 1 kHz and for operation at 256 kHz for Rnom = 150 K ohm load resistance and $f = \frac{256\ kHz}{2^n-1}$ where n = configuration number. The purpose here is to evaluate frequency performance at different load resistance conditions for operation in the 1st, 2nd, 3rd and 4th stage of cascade operation. The results are shown in Figs. 62-89 inclusive and specified in Table 19. It can be seen that speed capability of the circuit is in excess of that required in the NAS.. circuit "Basic MOSFET Blocks" #GD-1153-819. At the lowest value of load resistance examined, 150 kohm (nominal) maximum observed frequency of operation was ≥1.4 MHz. The low voltage operating capability was examined. It was found that most units ceased operation at about 2.0 volts peak to peak input signal. Values for a typical unit for each group are included in Table 19.

The circuit used for evaluating performance is shown in Fig. 90. Unfortunately this circuit does not rigorously satisfy the previously mentioned requirement that input voltage and its complement do not overlap in the negative direction. In a few cases this has been observed to result in a 1:1 input-output frequency correspondence and can be counteracted by slowing up the time constant of the output circuitry by adding some load capacitance. 10 pf or greater has in most cases been found sufficient. This problem is readily overcome by the use of two separate synchronously operated pulse generators to avoid the overlap condition.

In some instances, the negative waveform is seen to have a step in the base (Fig. 84). This is attributed to the onset of undesirable conduction due to threshold voltage differences. Counting efficiency, however, is not materially effected.



IN

$\overline{\text{IN}}$

OUT

$\overline{\text{OUT}}$

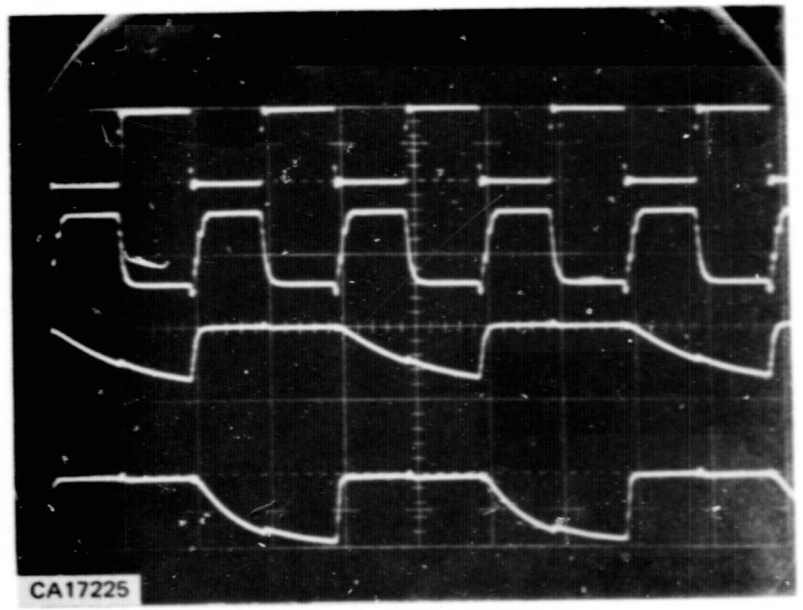
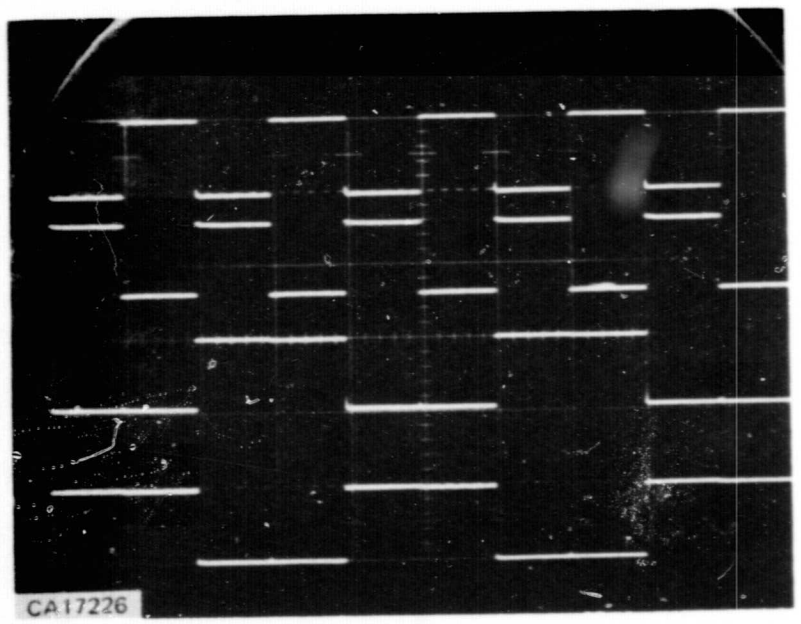


Figure 62. Circuit Operation, Unit No. 1, f = 1kHz

Figure 63. Circuit Operation, Unit No. 1, f = 256 kHz



IN

$\overline{\text{IN}}$

OUT

$\overline{\text{OUT}}$

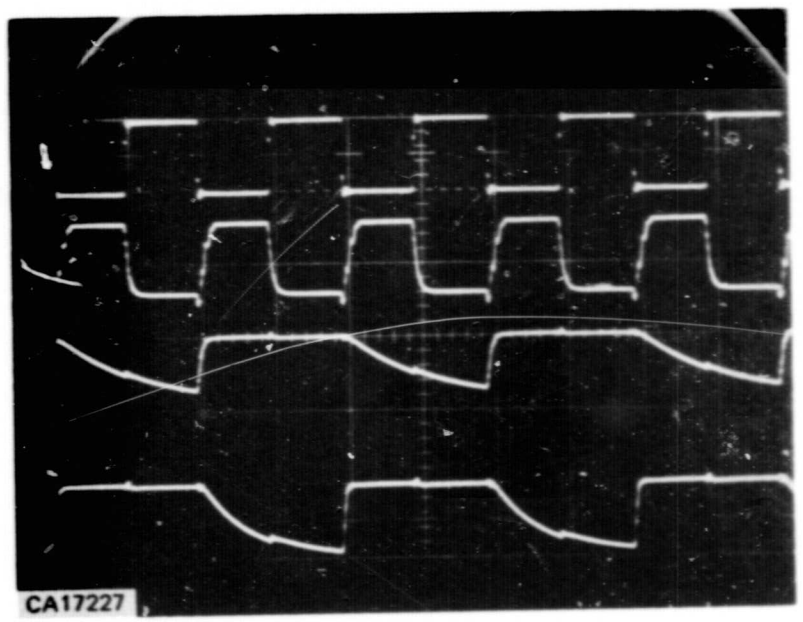


Figure 64. Circuit Operation, Unit No. 2, f = 1kHz

Figure 65. Circuit Operation, Unit No. 2, f = 256 kHz

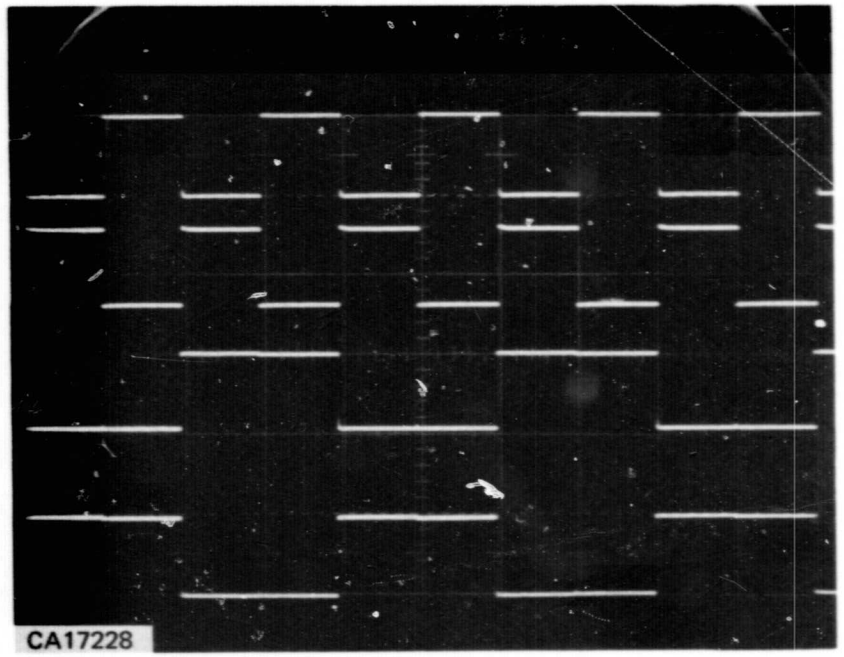


Figure 66. Circuit Operation, Unit No. 7, f = 1 kHz

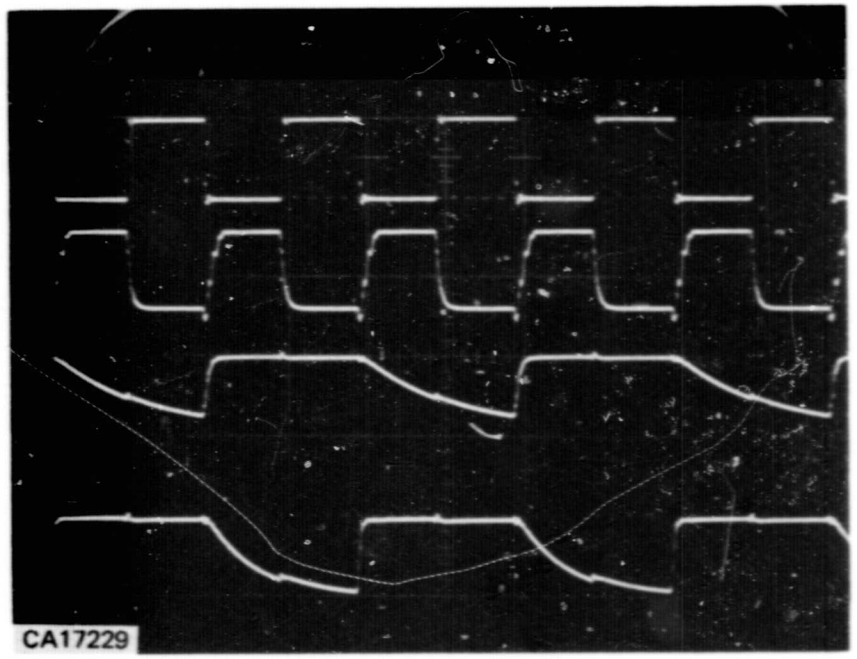


Figure 67. Circuit Operation, Unit No. 7, f=256 kHz

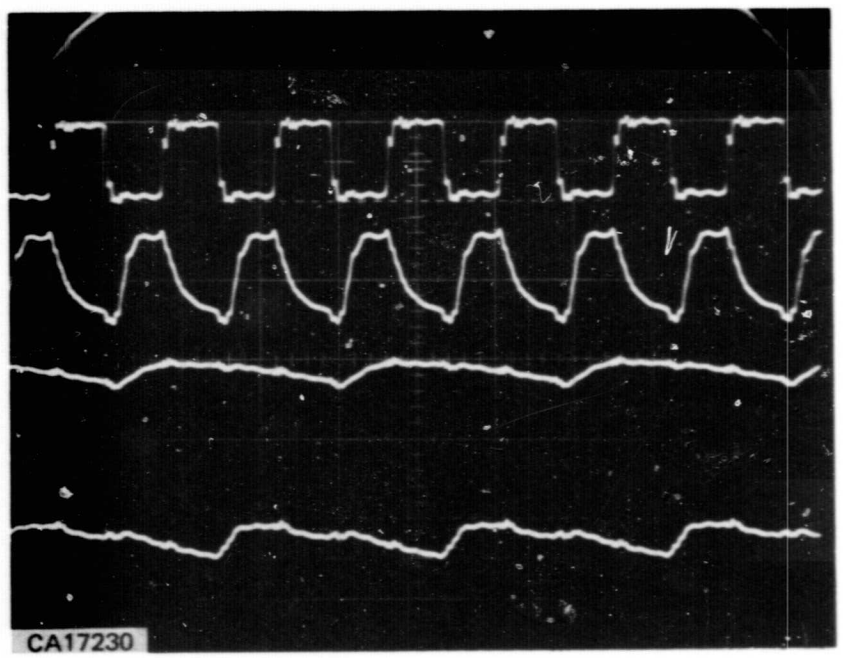


Figure 68. Circuit Operation, Unit No. 1, f=1400 kHz

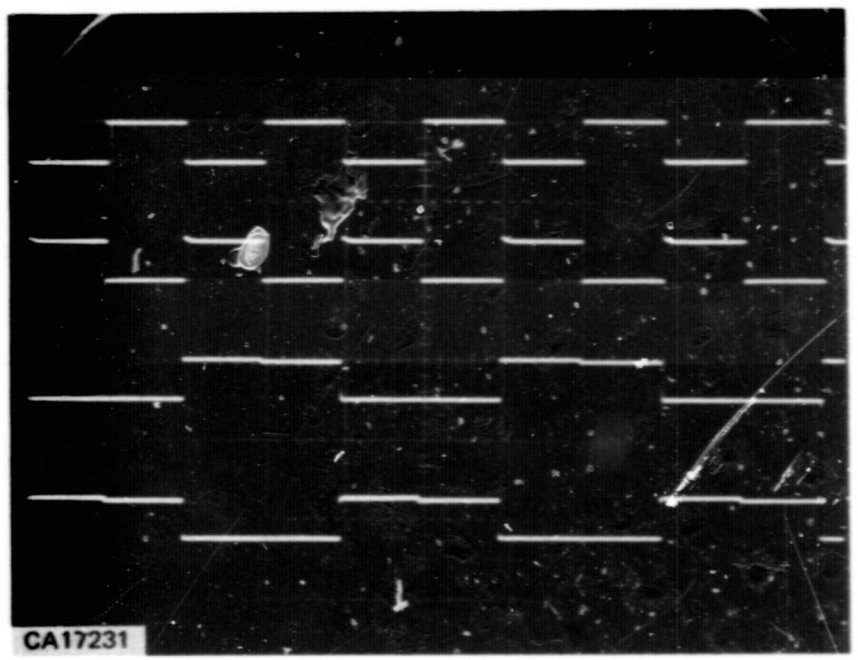
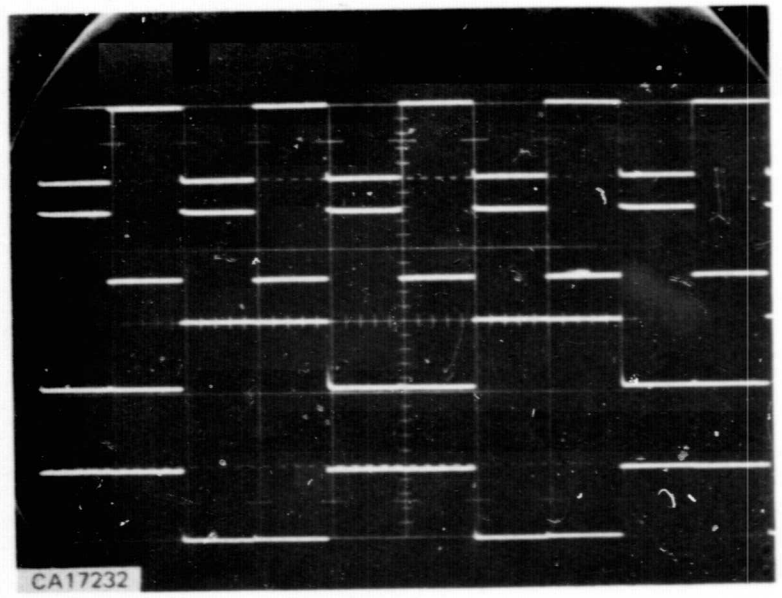


Figure 69. Circuit Operation, Unit No. 1, f = 1kHz (Min. Ampl.)



IN

$\overline{IN}$

OUT

$\overline{OUT}$

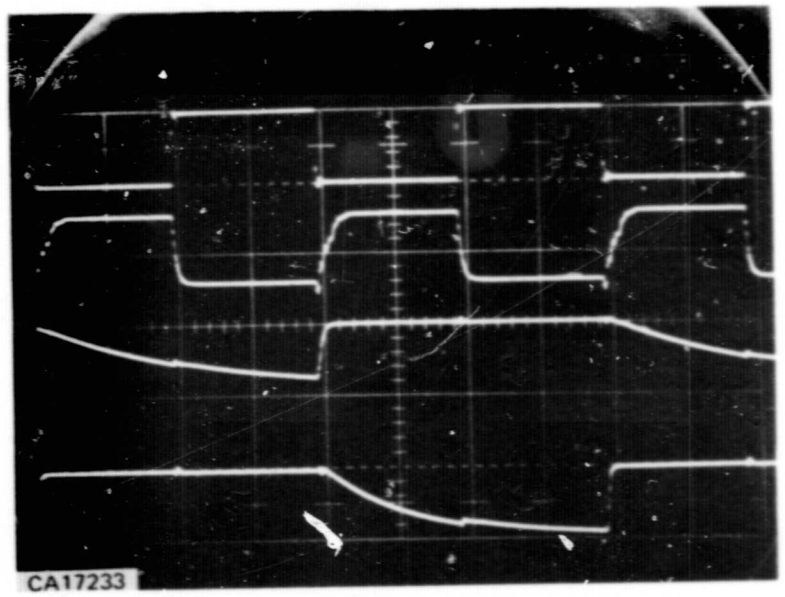
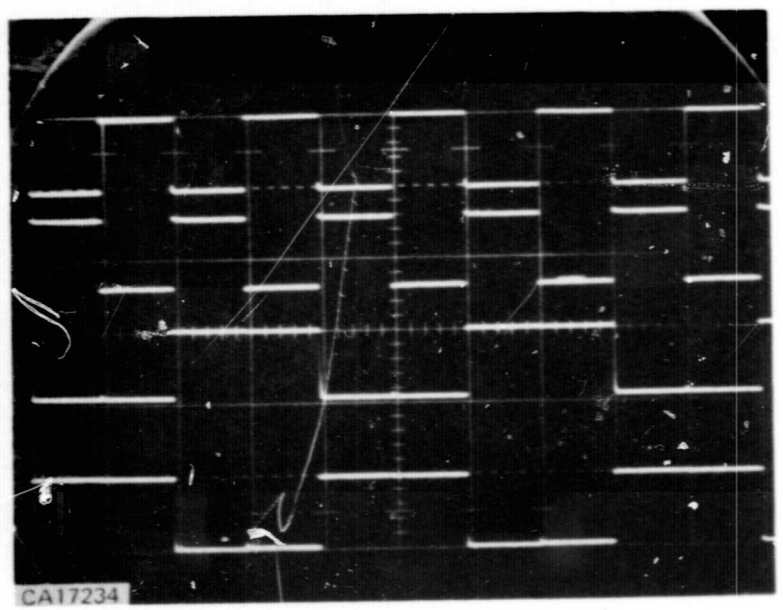


Figure 70. Circuit Operation, Unit No. 11, f=1 kHz

Figure 71. Circuit Operation, Unit No. 11, f=128 kHz



IN

$\overline{IN}$

OUT

$\overline{OUT}$

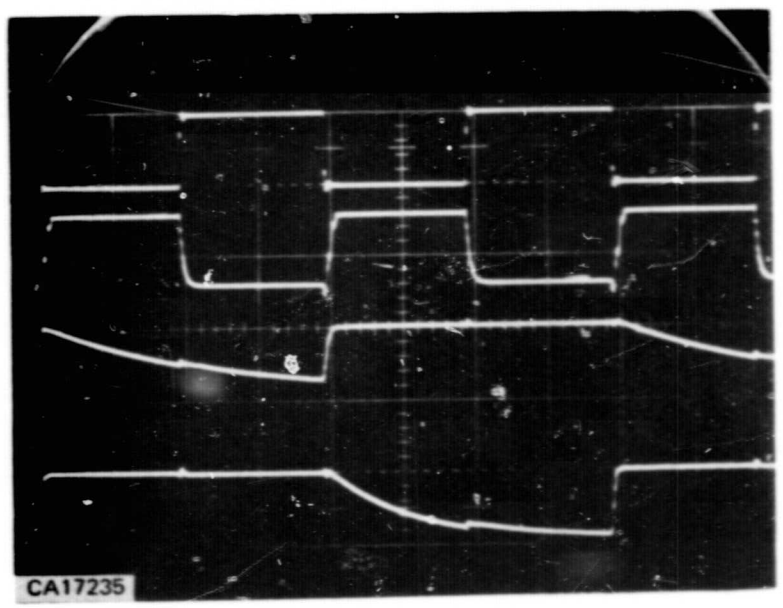


Figure 72. Circuit Operation, Unit No. 13, f=1 kHz

Figure 73. Circuit Operation, Unit No. 13, f=128 kHz

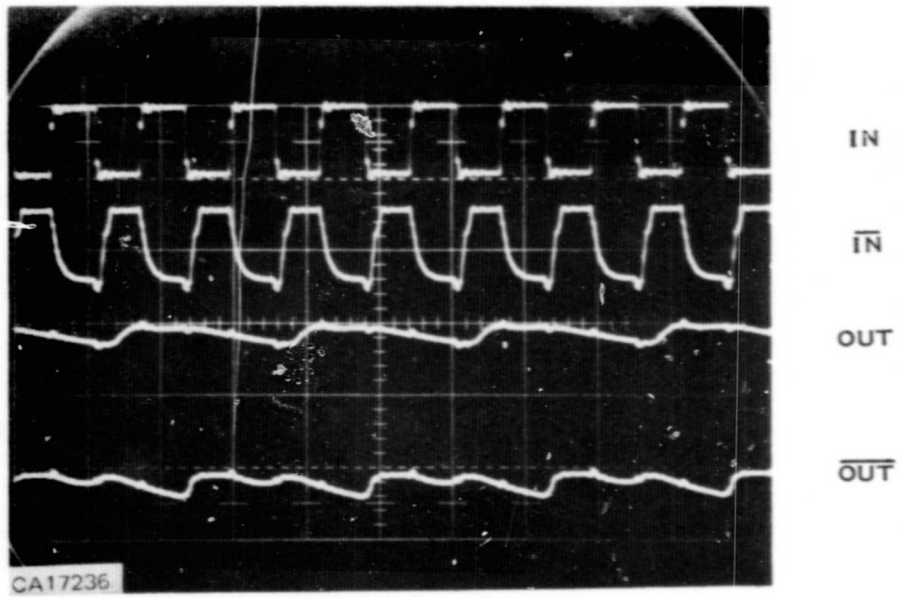


Figure 74. Circuit Operation, Unit No. 11, f = 800 kHz

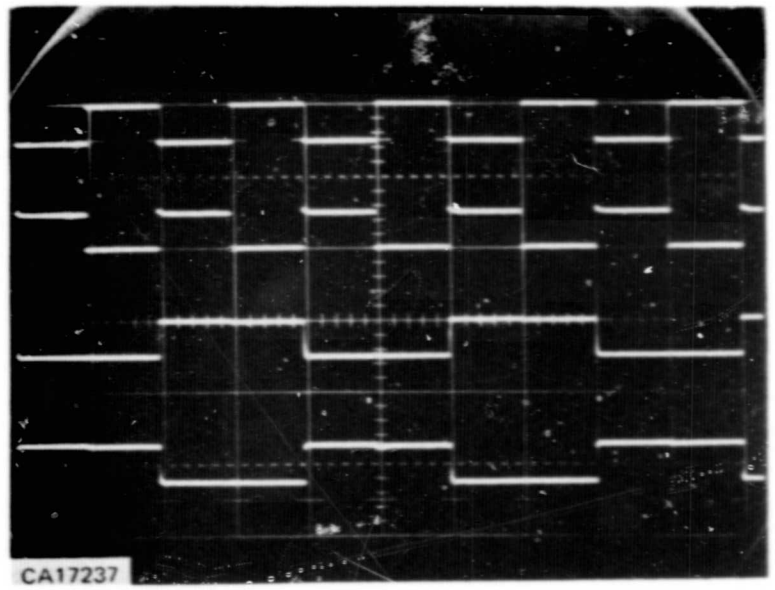


Figure 75. Circuit Operation, Unit No. 11 f = 1 kHz (Min. Ampl.)

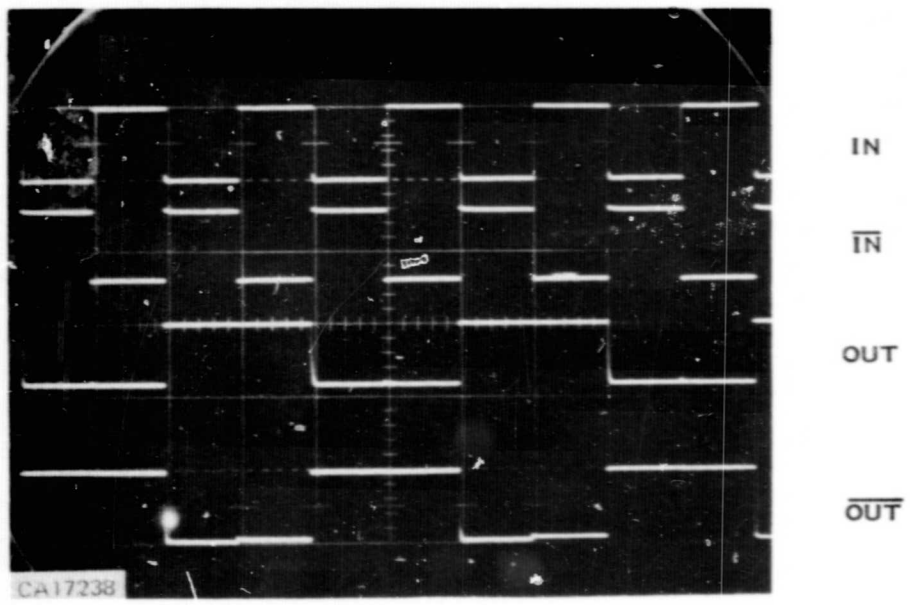


Figure 76. Circuit Operation, Unit No. 22, f = 1 kHz

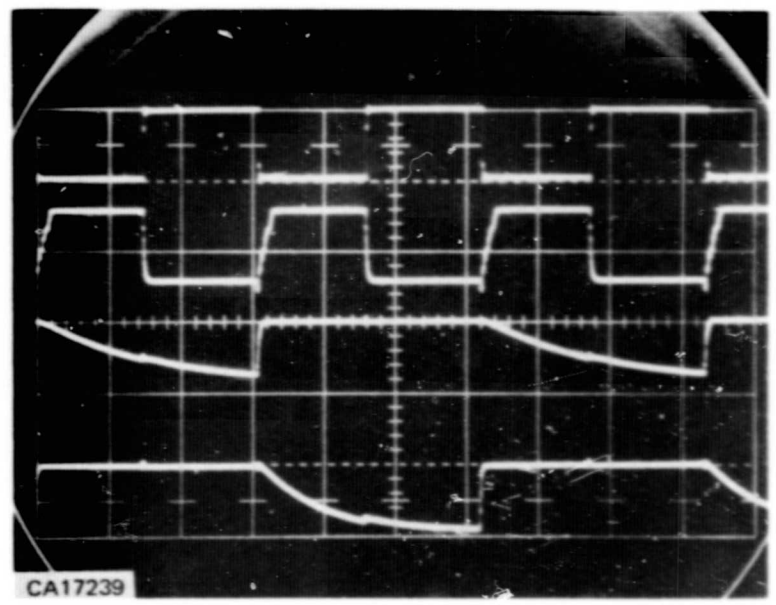
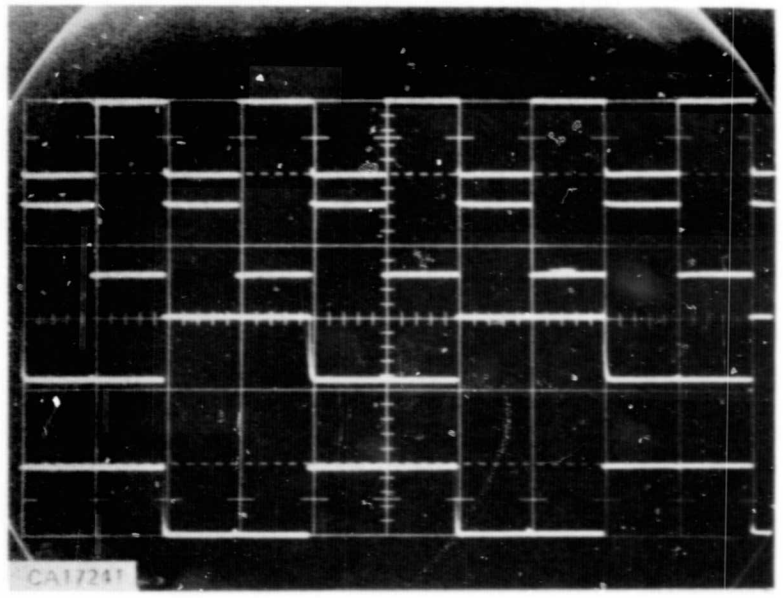


Figure 77. Circuit Operation, Unit No. 22, f = 64 kHz



IN

$\overline{IN}$

OUT

$\overline{OUT}$

Figure 78. Circuit Operation, Unit No. 25, f = 1 kHz

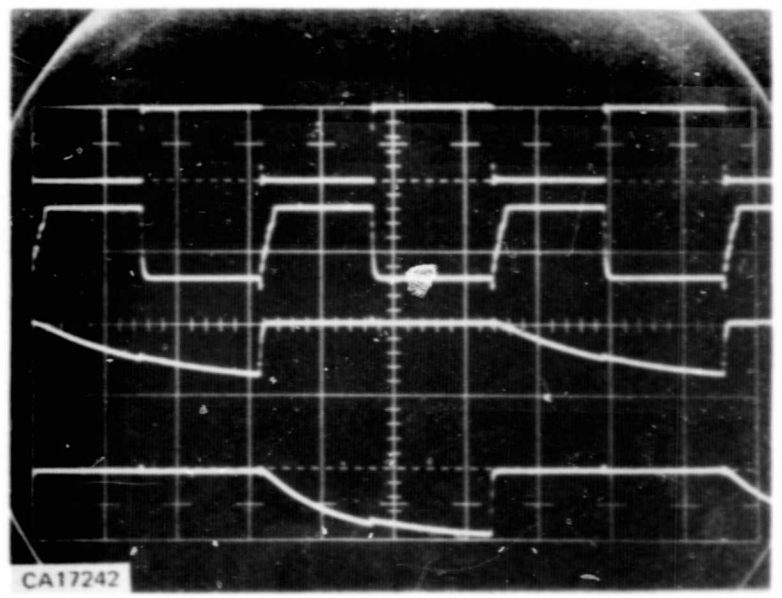
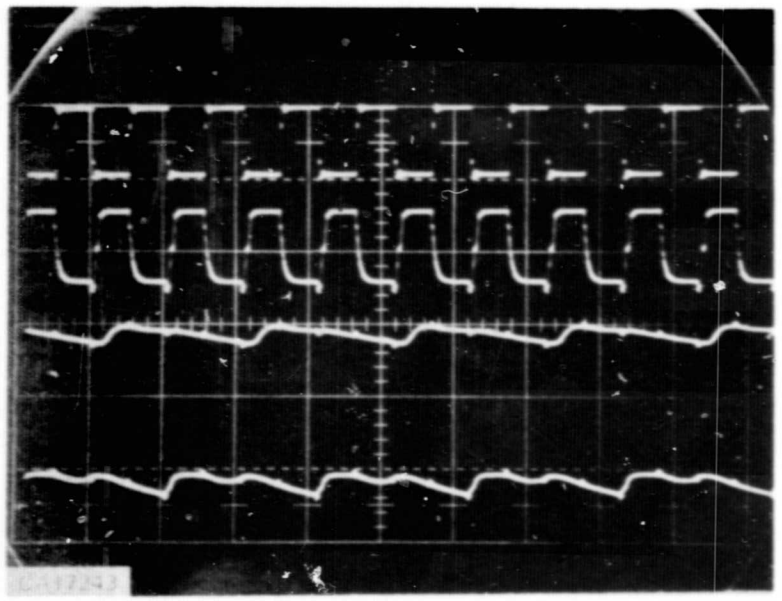


Figure 79. Circuit Operation, Unit No. 25, f = 64 kHz



IN

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OUT

$\overline{OUT}$

Figure 80. Circuit Operation, Unit No. 22, f = 500 kHz

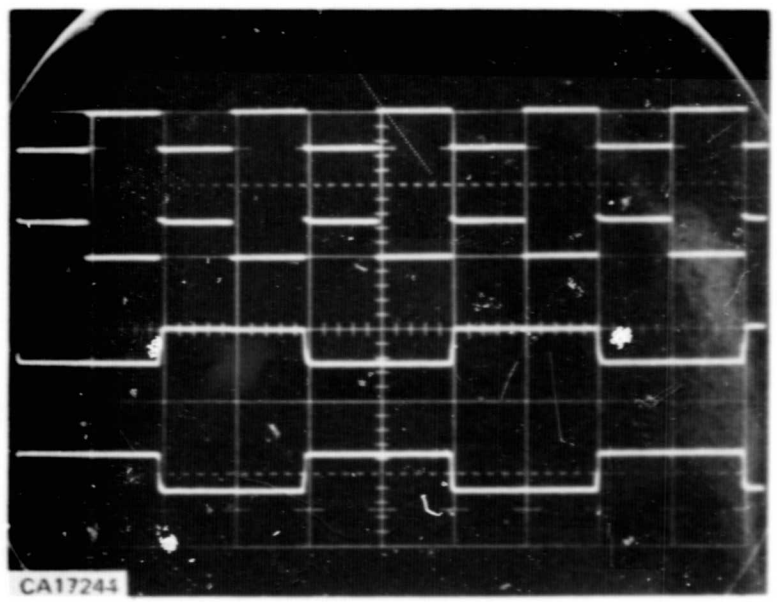
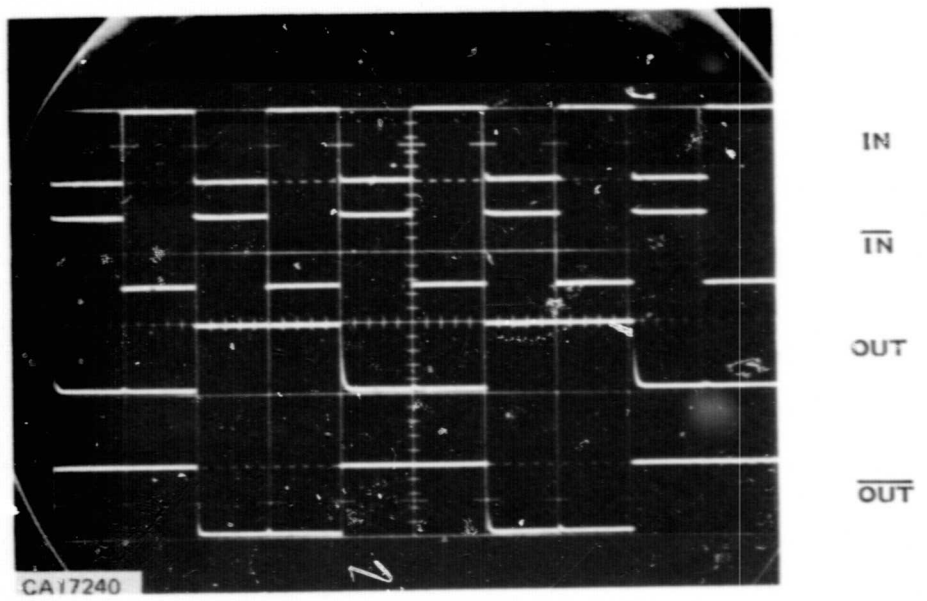


Figure 81. Circuit Operation, Unit No. 22, f = 1 kHz (Min. Ampl.)



IN

$\overline{\text{IN}}$

OUT

$\overline{\text{OUT}}$

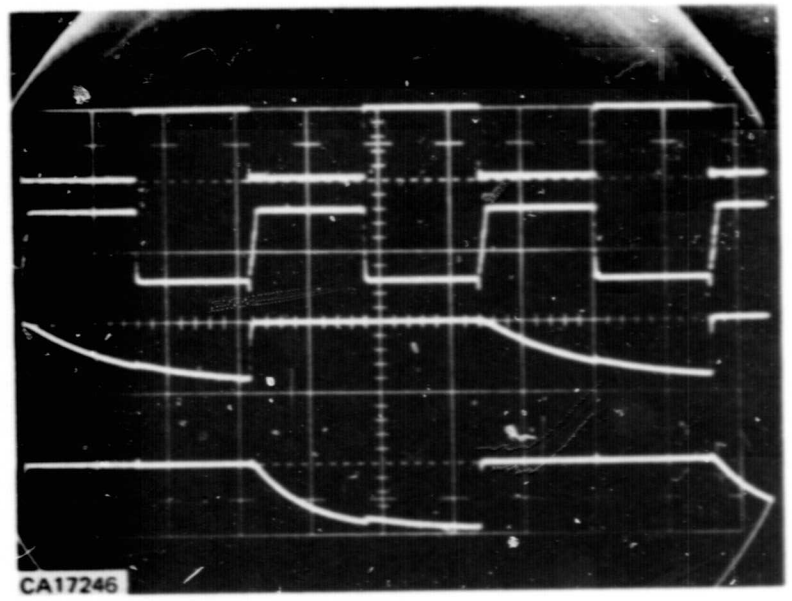
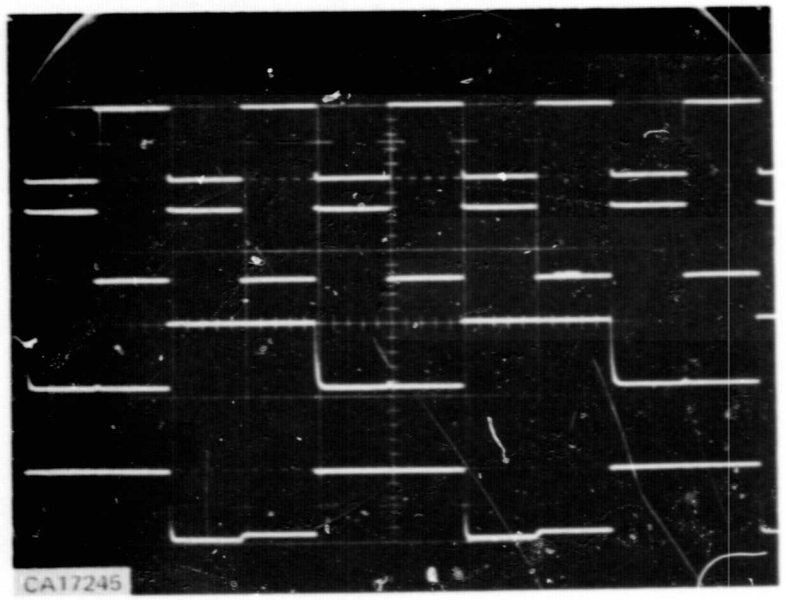


Figure 82. Circuit Operation, Unit No. 34, f = 1 kHz

Figure 83. Circuit Operation, Unit No. 34, f = 32 kHz



IN

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OUT

$\overline{\text{OUT}}$

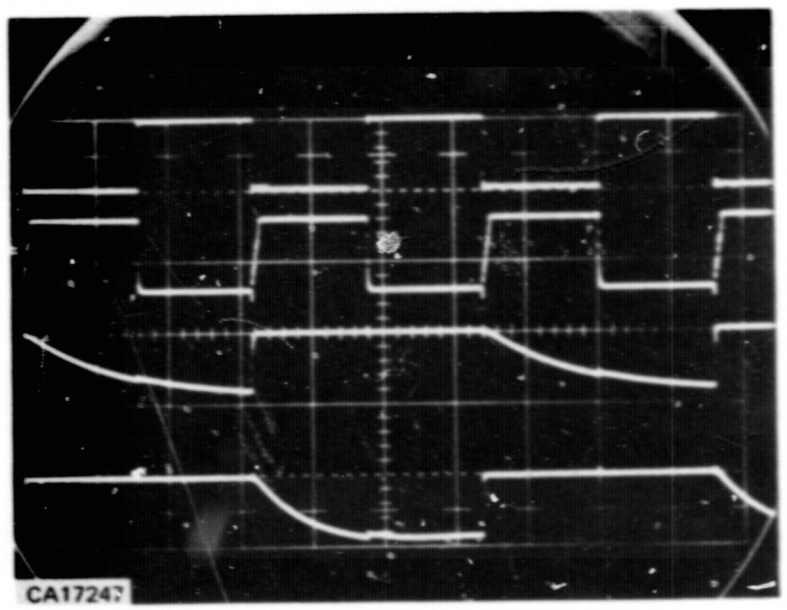

Figure 84. Circuit Operation, Unit No. 35, f = 1 kHz

Figure 85. Circuit Operation, Unit No. 35, f = 32 kHz

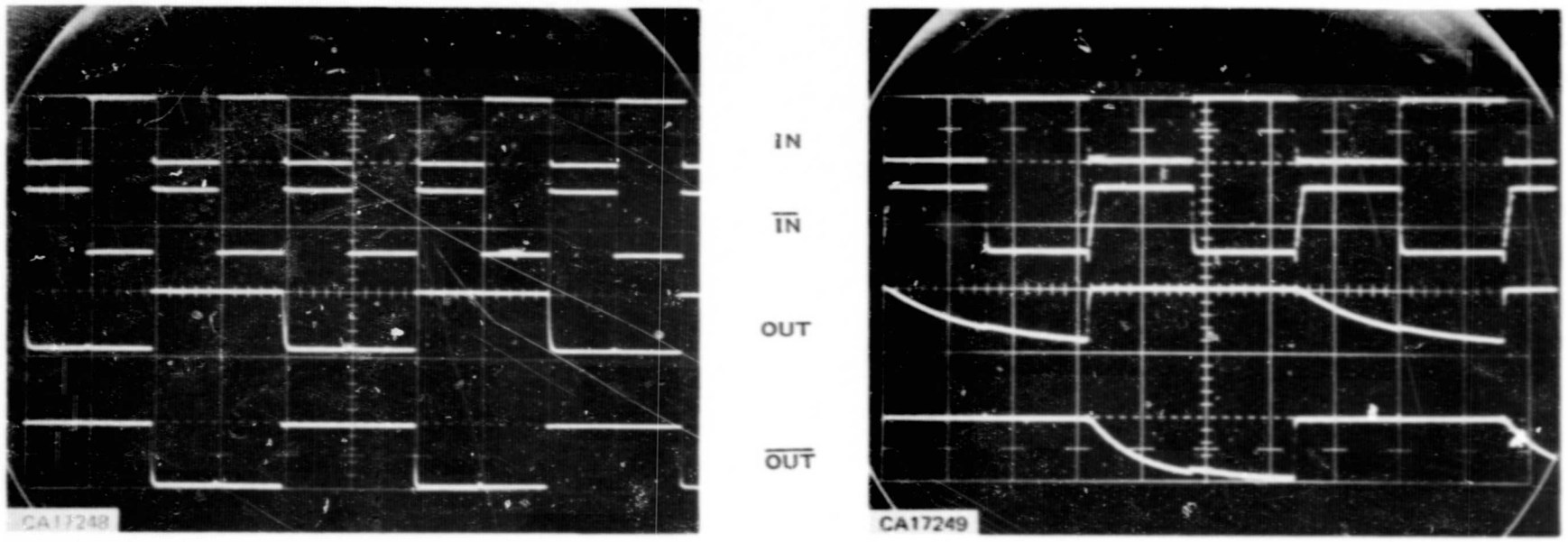

Figure 86. Circuit Operation, Unit No. 36, f = 1 kHz

Figure 87. Circuit Operation, Unit No. 36, f = 32 kHz

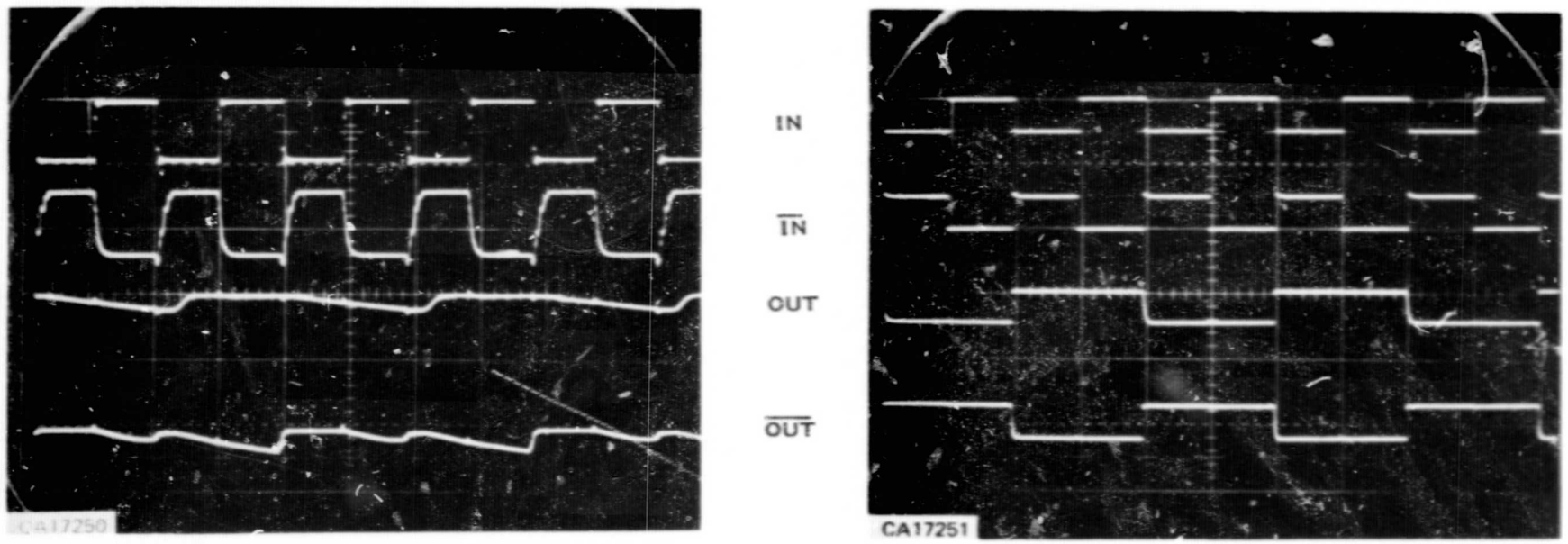

Figure 88. Circuit Operation, Unit No. 36, f = 264 kHz

Figure 89. Circuit Operation, Unit No. 36, f = 1 kHz (Min. Ampl.)

Table 19. Circuit Operating Conditions

Fig. #	Unit #	Time Scale (μsec/cm)	f (kHz)	Vertical Scale (V/cm)	Configuration #	
62	1	500	1	10	2	
63	1	2	256	10	2	
64	2	500	1	10	2	
65	2	2	256	10	2	
66	7	500	1	10	2	
67	7	2	256	10	2	
68	1	0.5	1400	10	2	Max. operating frequency
69	1	500	1	5	2	Min. amplitude ~2.0V
70	11	500	1	10	3	
71	11	2	128	10	3	
72	13	500	1	10	3	
73	13	2	128	10	3	
74	11	1	800	10	3	Max. operating frequency
75	11	500	1	5	3	Min. amplitude ~2.0V
76	22	500	1	10	4	
77	22	5	64	10	4	
78	25	500	1	10	4	
79	25	5	64	10	4	
80	22	2	500	10	4	Max. operating frequency
81	22	500	1	5	4	Min. amplitude ~2.3V
82	34	500	1	10	5	
83	34	10	32	10	5	
84	35	500	1	10	5	
85	35	10	32	10	5	
86	36	500	1	10	5	

Table 19. Circuit Operating Conditions (Cont)

Fig. #	Unit #	Time Scale (μsec/cm)	f (kHz)	Vertical Scale (V/cm)	Configuration #	
87	36	10	32	10	5	
88	36	2	264	10	5	Max. operating frequency
89	36	500	1	5	5	Min. amplitude ~2.0V

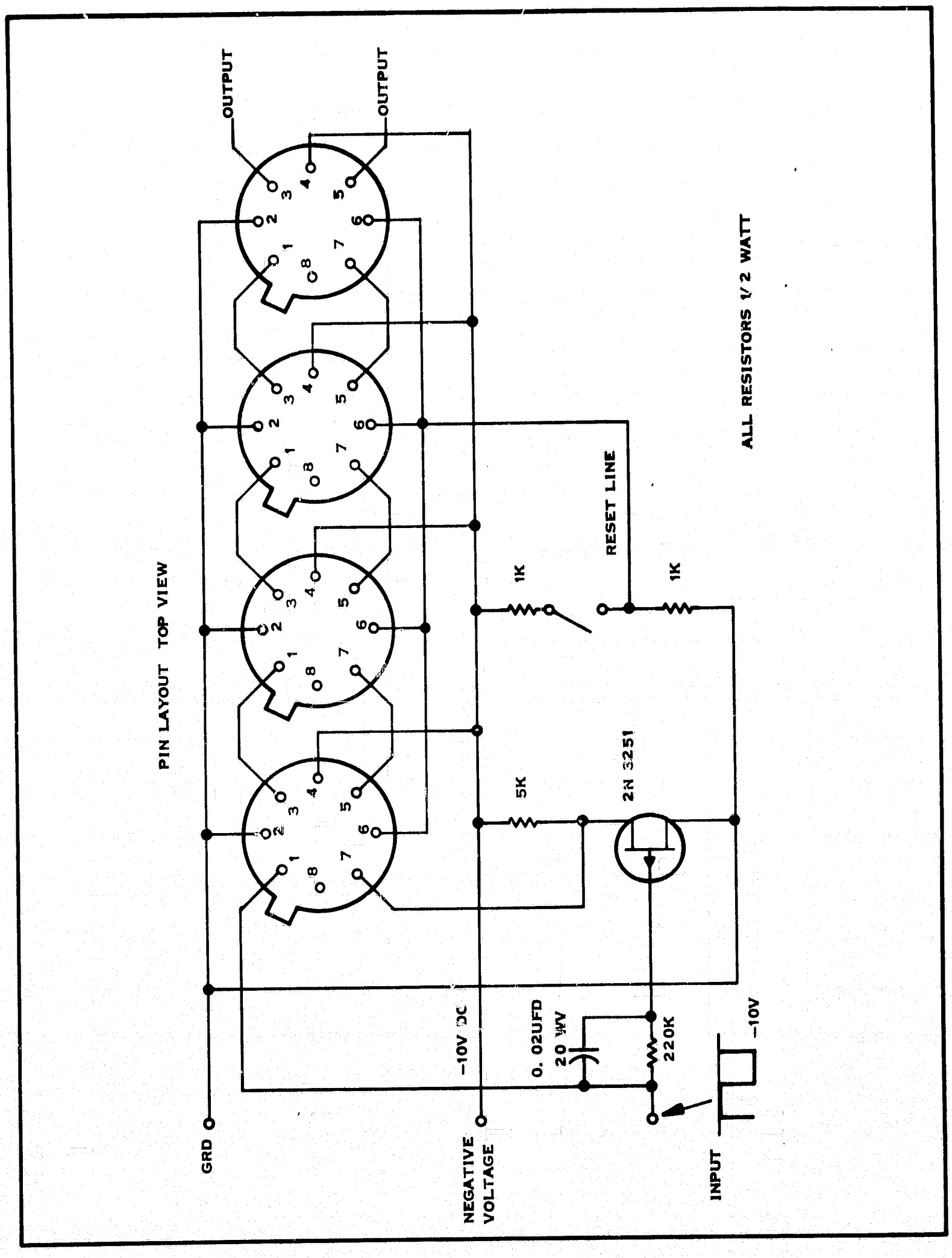

Figure 90. Schematic for Testing MNOSFET – CERMET Integrated Circuit Binary Converter

SECTION V

SUMMARY AND CONCLUSION

It has been demonstrated under this contract that MNOSFETs with appropriate thin film load resistors can be produced on a single chip by compatible processes. Early in the contract period discrete MNOSFETs produced by Texas Instruments were found to suffer less change in parameters after electron irradiation than MOSFETs previously tested. The MNOSFETs combined with cermet resistors in the binary counters produced under this contract have not been completely tested by NASA under electron irradiation, but will be a portion of a subsequent report by NASA. However, as stated in Section I of this report, discrete cermet resistors companion to those used as load resistors on the circuit when tested by NASA suffered no measureable degradation ($\leq 0.5\%$) after accumulative irradiation of 10^{15} e/cm^2 with a maximum flux of 10^{12} e/cm^2 -sec. John Tarpley believes these units to be among the most stable resistors of this range under this stress. From these brief statements, it is concluded that the major objectives of the revised program are complete.

The layout of the binary counter and load resistors did not make an effort to conserve area on the chip. It included multitapped resistors as well as four test MNOSFETs with different w/l ratios. A circuit intended for actual space vehicle application would use only the appropriate value of load resistor per element and would eliminate the large test transistor area. Circuits requiring other resistor values could be achieved by interspacing the various circuits in the step-repeat portion of the photomask array master. Such masking technology is widely available in the semiconductor industry.

The placement of the cermet thin film resistors on the same chip as the MNOSFET circuit elements should provide reliability advantages normally cited for Integrated Circuits in comparison with printed circuit boards using discrete soldered elements. On the particular circuit constructed under this contract, the use of cermet resistors should provide a functionspace saving of a factor of five over the circuit plus discrete load resistor case; it should also eliminate eight printed circuit board connections per chip. Of course much more complicated elements than this simple binary counter

could be achieved with this technology, producing an even greater space saving and greater reliability.

The processing technology utilized in the MNOSFET-cermet circuit unquestionably requires more process steps by the semiconductor manufacturer than a simple MOSFET circuit with external resistors. The cermet process after contact apertures are formed requires:

(1) Evaporation of aluminum
(2) Removal of the aluminum into a reverse resistor pattern, using a photolithographic process
(3) Deposition of the cermet
(4) Etching of the cermet

These steps are followed by contact application and an annealing step not unlike conventional circuits. Individual readers may apply their normal costs for such processes to calculate the increase in cost of the circuit. The silicon nitride portion of the process may well be vital to the use of cermet resistors while maintaining MISFET reliability, since it supplies an ion barrier during processing. Ordinary silicon oxide protected devices usually fail to passivate against such processing. Further it is the opinion of the authors that MNOSFET processing for highly stable elements is easier than the use of clean or phosphorus doped oxides and electron beam evaporated clean contacts. This statement assumes that quantity production techniques for surface preparation and silicon nitride application have reached a developed state. Once the device is coated with silicon nitride the device is fairly tolerant to further processing; in particular it is a barrier to sodium migration from the outer surface. This is of course not true for the silicon dioxide-device counterpart.

Based on what is known at Texas Instruments about silicon nitride and clean oxide formation techniques, it is the cermet resistor yield that will dominate in device cost considerations for the very high resistance, zero temperature coefficient resistors. If a high yield procedure is developed for the cermet, the cost of an MNOSFET circuit with cermet load resistors should not exceed by more than a factor of 1.5-2.0x that of an MOSFET circuit produced in comparable volume. After some two to five years it is speculated that MNOSFET or alumina replacement for the silicon nitride MISFETs circuits may be less costly than their simple doped oxide counterparts. Further the higher performance circuits achieveable with such technology should force its acceptance. In any case if continued studies of the radiation tolerance of MNOSFET-cermet

resistor structures remain favorable, this technology or its equivalent should be required by NASA simply on the basis of system reliability lifetime in space flight.

SECTION VI

SOME SUGGESTED WORK

Much required work is evident over that described in this report. At the present time a sufficient quantity of circuits could be made for a complex system using the laboratory processes described in this report. Yields could be kept reasonable through running pilot structures to ensure material properties, and interspersing circuit runs with test structures. Such systems would be costly but could be achieved immediately. System reliability would have to be determined through a step stress program including mechanical testing.

For a true manufacturing system, a technique such as flash evaporation or sputtering is suggested for cermet formation. As noted in the text, the evaporation procedure used in this contract most likely produced a graded composition structure to yield a sheet resistance-temperature coefficient combination not achieved in the literature reviewed. However, for most MISFET circuits, the stringent temperature coefficient requirement of this contract is probably not required. Hence a cermet technique yielding homogeneous composition is likely satisfactory. In addition large quantity silicon nitride coating equipment will be necessary along with clean oxide techniques.

It is suggested that techniques for direct etching of the cermet, rather than the aluminum undercutting technique should be further investigated. While some brief examination of other etchants was made, the technique described was found capable of producing resistors of 0.4 mil width and 80 mils in length with good definition. Resistors separation capability of 0.4 mil was demonstrated with the use of a repeated T-type pattern. Hence, no further development was attempted.

It is widely recognized in the lieterature that temperature-ambient effects can have a profound influence on the properties of the cermet. It would be of interest to see if over coating the cermet with a sputtered quartz layer or dielectric formed by low temperature chemical deposition would protect against such effects.

While other cermets can be produced it is suggested that the properties of the chromium-silicon monoxide formed cermet show adequate properties with reference to physical parameters, device processing, and reliability to suggest a concerted effort to reduce this material to a well qualified film for use on NASA circuits. Sputtered contact systems, beam leads, other insulators for substrates, and resistance trimming techniques could form the basis for such a study.

Since silicon nitride has been found useful with respect to electron irradiation tolerance, aluminum oxide films prepared by chemical techniques are also of interest. It has already been reported that aluminum oxide films formed by gaseous anodization for use on MISFETs offer great radiation tolerance. Aluminum oxide films deposited by chemical techniques at Texas Instruments have been used on MISFETs and have shown 300°C stress reliability under $\pm 10^6$ v/cm within 0.2 v over 100 hours. Very low value negative to positive threshold voltages can be obtained with these films, which suggests sophisticated circuit applications are possible. These higher speed circuits could in many cases make good use of cermet high value resistors. The compatibility of the technology and its radiation dependence have not been demonstrated.

A final suggestion made for future work is to investigate the more fundamental properties of the dielectrics and resistors in a form not protected from the electron irradiation by a metal can. In particular it is of interest to determine what effect electron irradiation has on units protected only by glass films or polymeric materials such as RTV. The transistors used for test pruposes on the binary counter could have been used for this purpose, although their geometry is too small to make accurate measurements of fundamental physical parameters possible.

SECTION VII

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